

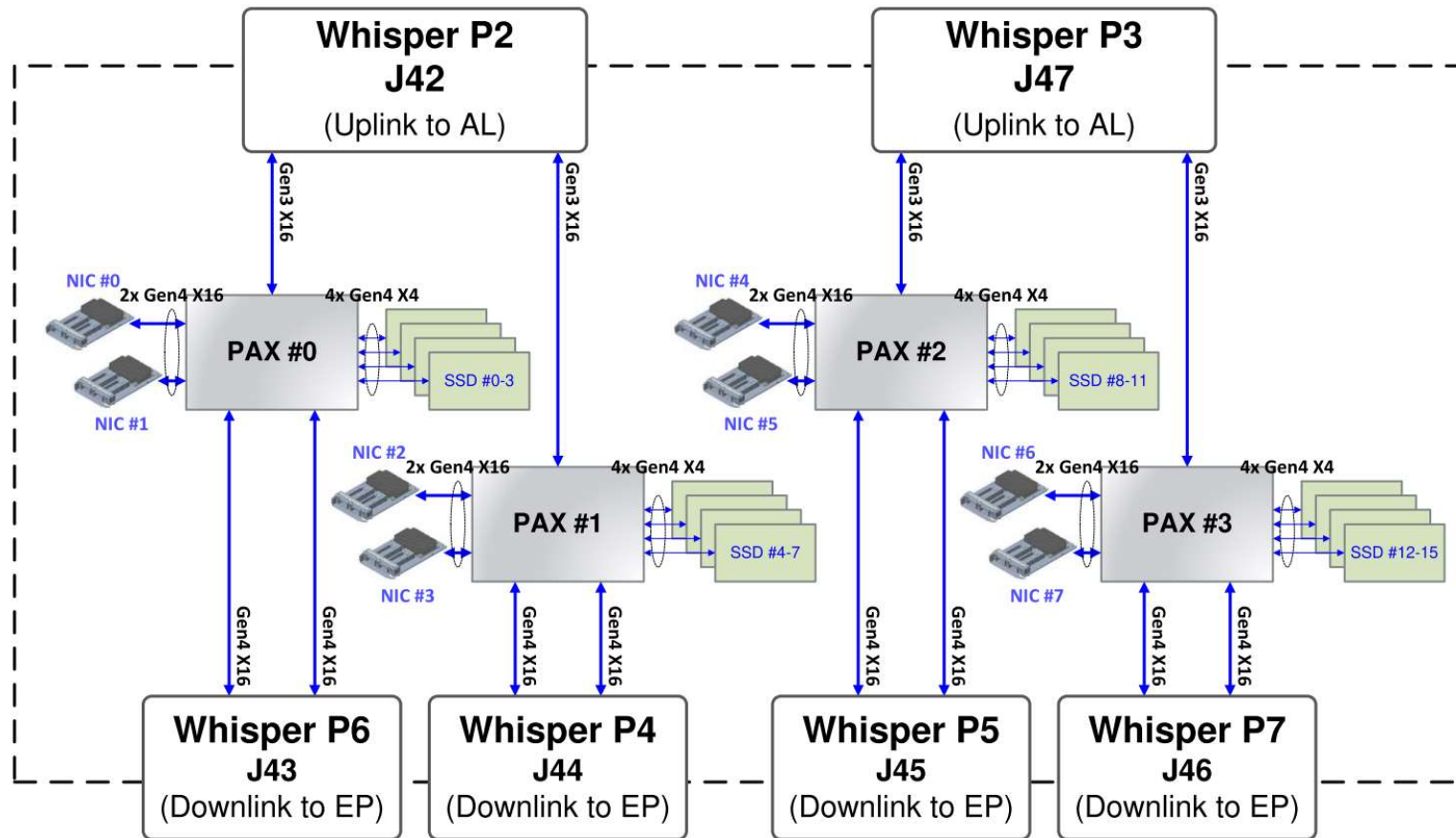
BASEBOARD

001 CORVER PAGE
002 TABLE OF CONTENT
003 SYSTEM DIAGRAM
004 POWER SEQUENCE
005 CLOCK DIAGRAM
006 I2C Topology
007 USB TOPOLOGY
008 JTAG Diagram
009 BLANK
010 BLANK
011 PAX_STRAPS
012 PAX0_STATION_0_1
013 PAX0_STATION_2_3
014 PAX0_STATION_4_5
015 PAX0_GPIO
016 PAX0_PWR_GND(1/3)
017 PAX0_PWR_GND(2/3)
018 PAX0_PWR_GND(3/3)
019 PAX1_STATION_0_1
020 PAX1_STATION_2_3
021 PAX1_STATION_4_5
022 PAX1_GPIO
023 PAX1_PWR_GND(1/3)
024 PAX1_PWR_GND(2/3)
025 PAX1_PWR_GND(3/3)
026 PAX2_STATION_0_1
027 PAX2_STATION_2_3
028 PAX2_STATION_4_5
029 PAX2_GPIO
030 PAX2_PWR_GND(1/3)
031 PAX2_PWR_GND(2/3)
032 PAX2_PWR_GND(3/3)
033 PAX3_STATION_0_1
034 PAX3_STATION_2_3
035 PAX3_STATION_4_5
036 PAX3_GPIO
037 PAX3_PWR_GND(1/3)
038 PAX3_PWR_GND(2/3)
039 PAX3_PWR_GND(3/3)
040 CLOCK_GEN_100M
041 CLOCK_COMMON
042 CLOCK_GEN_9FGL04
043 CLK_BUFFER_DB2001
044 CKMNG
045 BLANK
046 USB_HUB_MB0
047 USB_HUB_MB1
048 USB_HUB_BMC
049 PAX_DEBUG_UART
050 PAX_UART_BUFFER

051 BMC_I2C_MUX
052 PAX_THERMAL_SENSOR
053 PAX_ISOLATION(1/2)
054 PAX_ISOLATION(2/2)
055 FLASH_MUX_G1 & G2
056 BASEBOARD_FRU_TEMP_SENSOR
057 BMC_IO_EXP
058 BMC_ADC(1/2)
059 BMC_ADC(2/2)
060 BMC_01
061 BMC_02
062 BMC_03
063 BMC_04
064 BMC_HW_STRAPPING_1
065 BMC_HW_STRAPPING_2
066 BMC_DDRIII_IV_SDRAM
067 BMC_NCSI
068 BLANK
069 BMC_CPLD_PULL_UP
070 M.2_CONNECTOR
071 BLANK
072 PFR_CPLD(1/6)
073 PFR_CPLD(2/6)
074 PFR_CPLD(3/6)
075 PFR_CPLD(4/6)
076 PFR_CPLD(5/6)
077 PFR_CPLD(6/6)
078 PFR_SPI
079 BLANK
080 FRONT_PANNEL_SLIMSAS_CONN
081 USB_DEBUG
082 PWR_CONN
083 SMBUS_REPEATER(1/3)
084 SMBUS_REPEATER(2/3)
085 SMBUS_REPEATER(3/3)
086 BLANK
087 I2C_RTC_IC
088 BMC&CPLD_DEBUG_HEADER
089 BLANK
090 TPM
091 WHISPER_ISO_UPLINK(1/2)
092 WHISPER_ISO_UPLINK(2/2)
093 WHISPER_ISO_DOWNLINK(1/2)
094 WHISPER_ISO_DOWNLINK(2/2)
095 BLANK
096 BLANK
097 BLANK
098 WHISPER_CONN0(1/2)
099 WHISPER_CONN0(2/2)
100 WHISPER_CONN1(1/2)

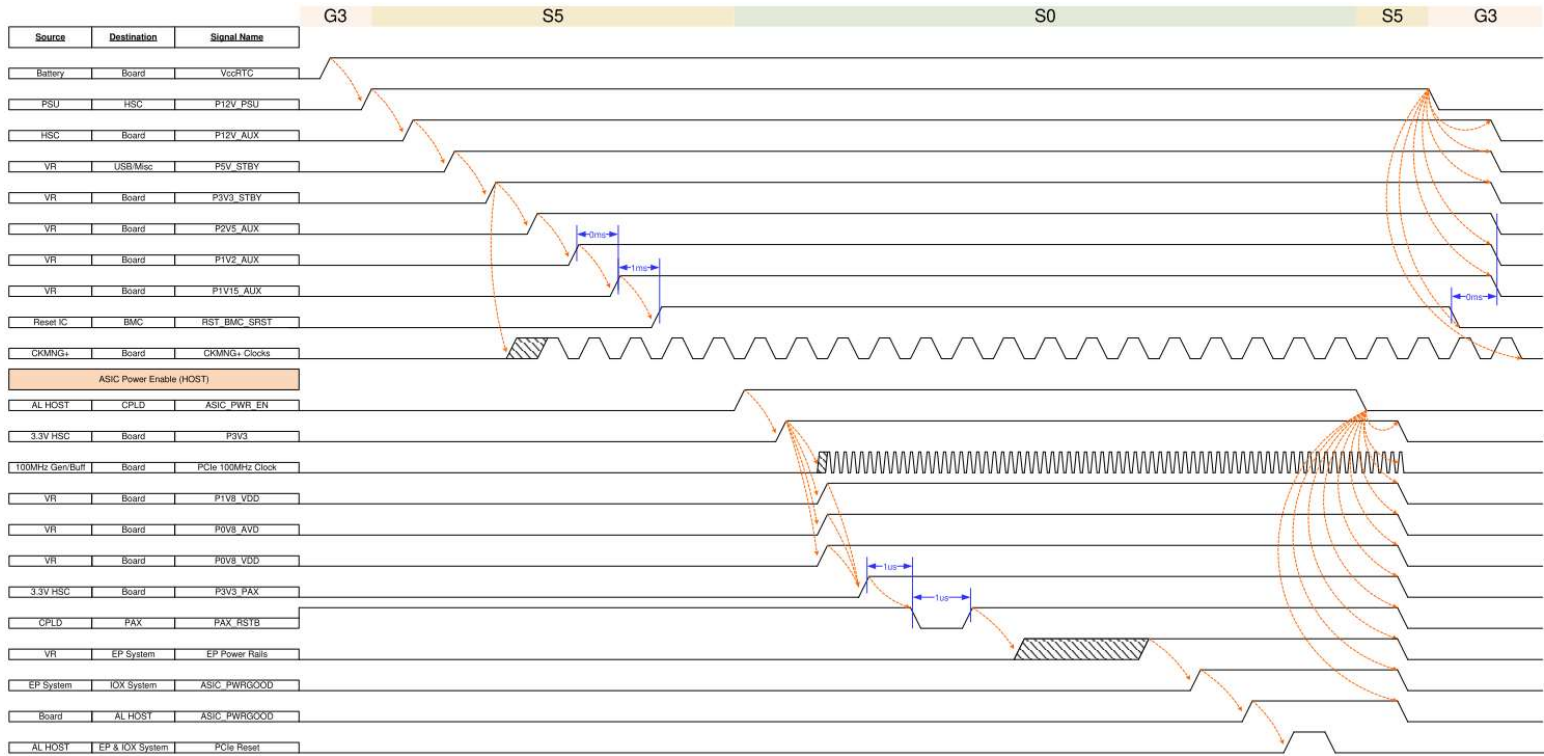
101 WHISPER_CONN1(2/2)
102 WHISPER_CONN2(1/2)
103 WHISPER_CONN2(2/2)
104 WHISPER_CONN3(1/2)
105 WHISPER_CONN3(2/2)
106 WHISPER_CONN4(1/2)
107 WHISPER_CONN4(2/2)
108 WHISPER_CONN5(1/2)
109 WHISPER_CONN5(2/2)
110 PCIE_OCP_V3.0_0(1/3)
111 PCIE_OCP_V3.0_0(2/3)
112 PCIE_OCP_V3.0_0(3/3)
113 PCIE_OCP_V3.0_1(1/3)
114 PCIE_OCP_V3.0_1(2/3)
115 PCIE_OCP_V3.0_1(3/3)
116 PCIE_OCP_V3.0_2(1/3)
117 PCIE_OCP_V3.0_2(2/3)
118 PCIE_OCP_V3.0_2(3/3)
119 PCIE_OCP_V3.0_3(1/3)
120 PCIE_OCP_V3.0_3(2/3)
121 PCIE_OCP_V3.0_3(3/3)
122 PCIE_OCP_V3.0_4(1/3)
123 PCIE_OCP_V3.0_4(2/3)
124 PCIE_OCP_V3.0_4(3/3)
125 PCIE_OCP_V3.0_5(1/3)
126 PCIE_OCP_V3.0_5(2/3)
127 PCIE_OCP_V3.0_5(3/3)
128 PCIE_OCP_V3.0_6(1/3)
129 PCIE_OCP_V3.0_6(2/3)
130 PCIE_OCP_V3.0_6(3/3)
131 PCIE_OCP_V3.0_7(1/3)
132 PCIE_OCP_V3.0_7(2/3)
133 PCIE_OCP_V3.0_7(3/3)
134 BLANK
135 BLANK
136 BLANK
137 BLANK
138 PCIE_NVMe_0(1/2)
139 PCIE_NVMe_0(2/2)
140 PCIE_NVMe_1(1/2)
141 PCIE_NVMe_1(2/2)
142 PCIE_NVMe_2(1/2)
143 PCIE_NVMe_2(2/2)
144 PCIE_NVMe_3(1/2)
145 PCIE_NVMe_3(2/2)
146 THROTTLE(1/2)
147 THROTTLE(2/2)
148 BLANK
149 P12V_OCP_V3 (1)
150 P12V_OCP_V3 (2)

151 P3V3_OCP_V3 (1)
152 P3V3_OCP_V3 (2)
153 P12V_NVME
154 P3V3_NVME
155 VR_P5V_STBY
156 VR_P3V3_STBY
157 VR_P2V5_AUX
158 VR_P1V15_AUX
159 VR_P1V2_AUX
160 VR_P1V8_VDD0_1
161 VR_P1V8_VDD2_3
162 VR_P0V8_VDD0
163 VR_P0V8_VDD1
164 VR_P0V8_VDD2
165 VR_P0V8_VDD3
166 VR_P0V8_AVD_PCIE0
167 VR_P0V8_AVD_PCIE1
168 VR_P0V8_AVD_PCIE2
169 VR_P0V8_AVD_PCIE3
170 P3V3/P3V3_PAX
171 TDR
172 DELTA_L
173 SCREW_HOLE
174 DUMMY_SYMBOL

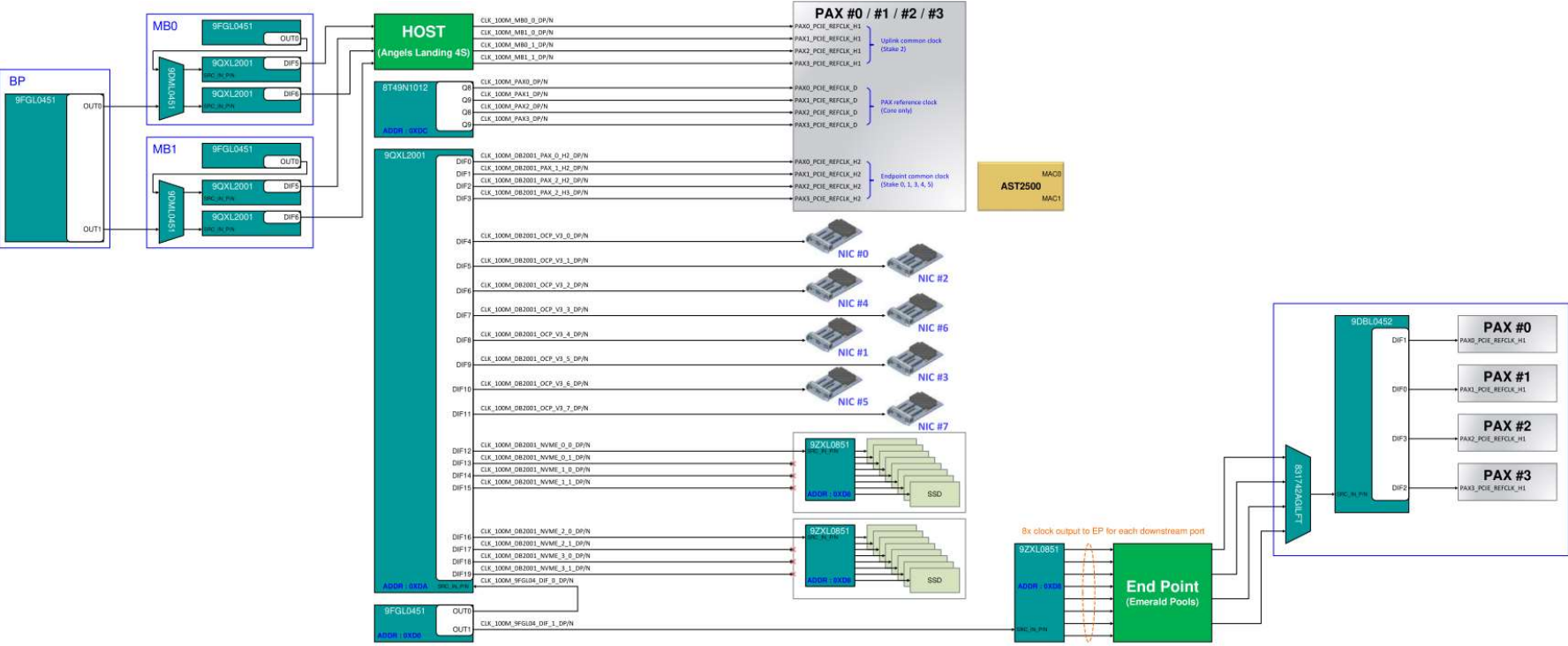


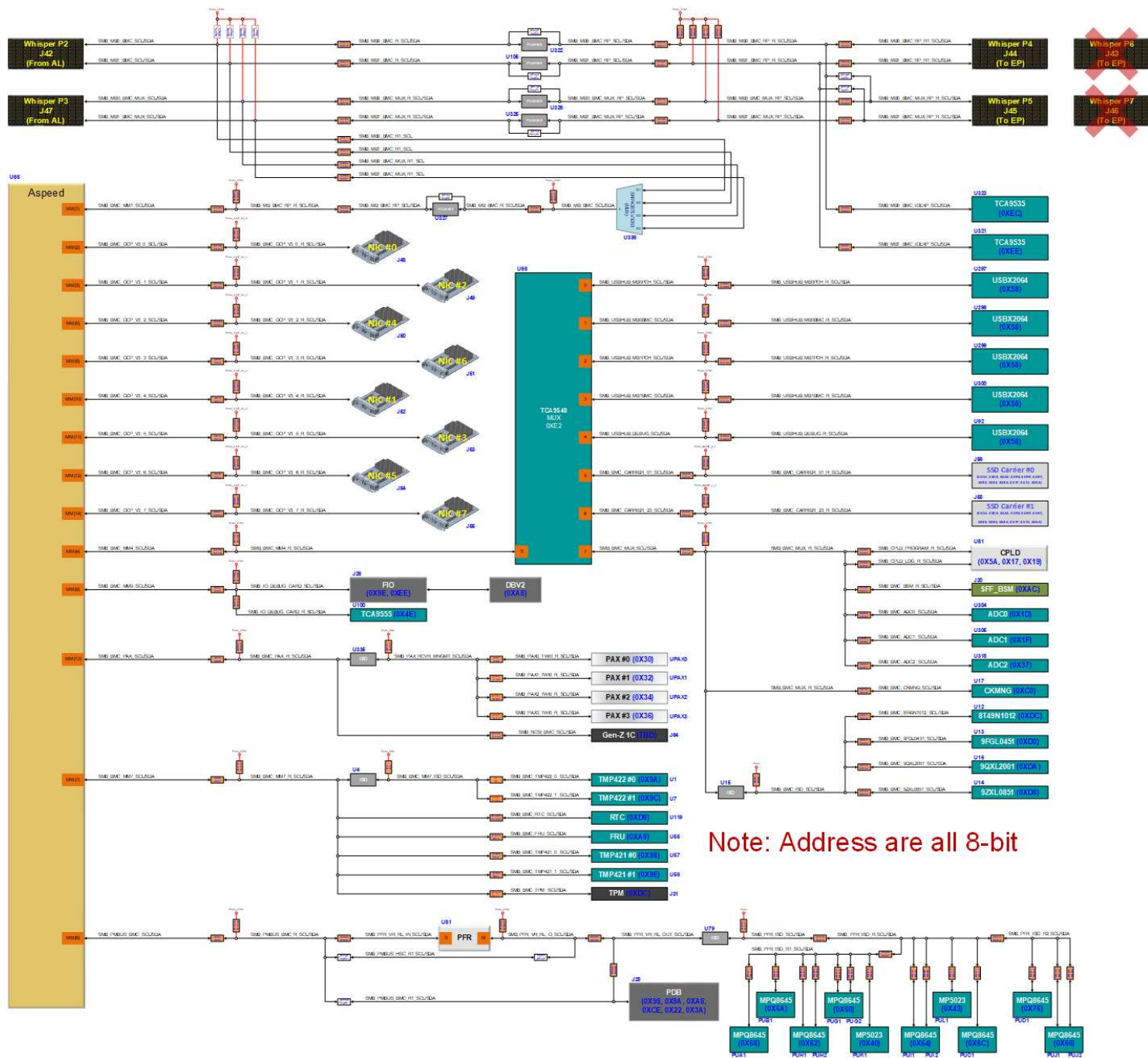
SYSTEM DIAGRAM

POWER SEQUENCE



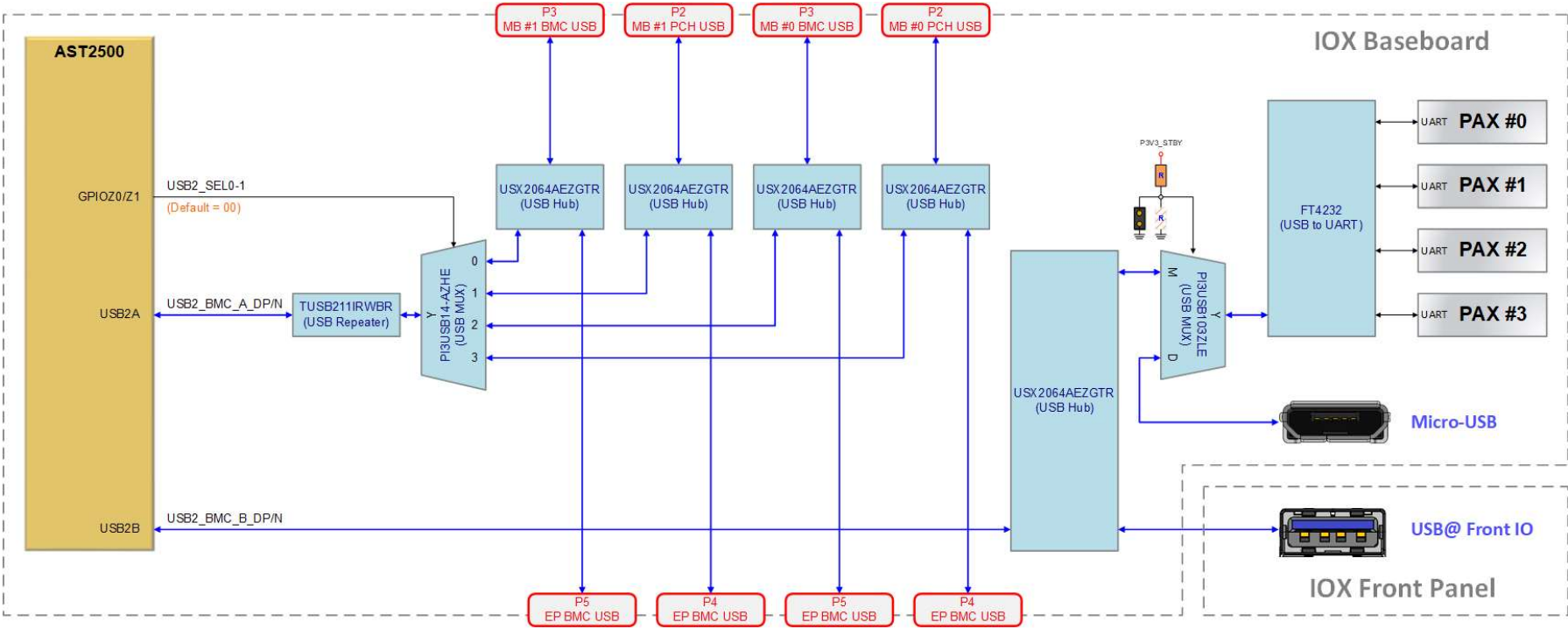
CLOCK DIAGRAM





I2C Topology

USB TOPOLOGY



BLANK

BLANK

17.1.3 Bootstrap Pins

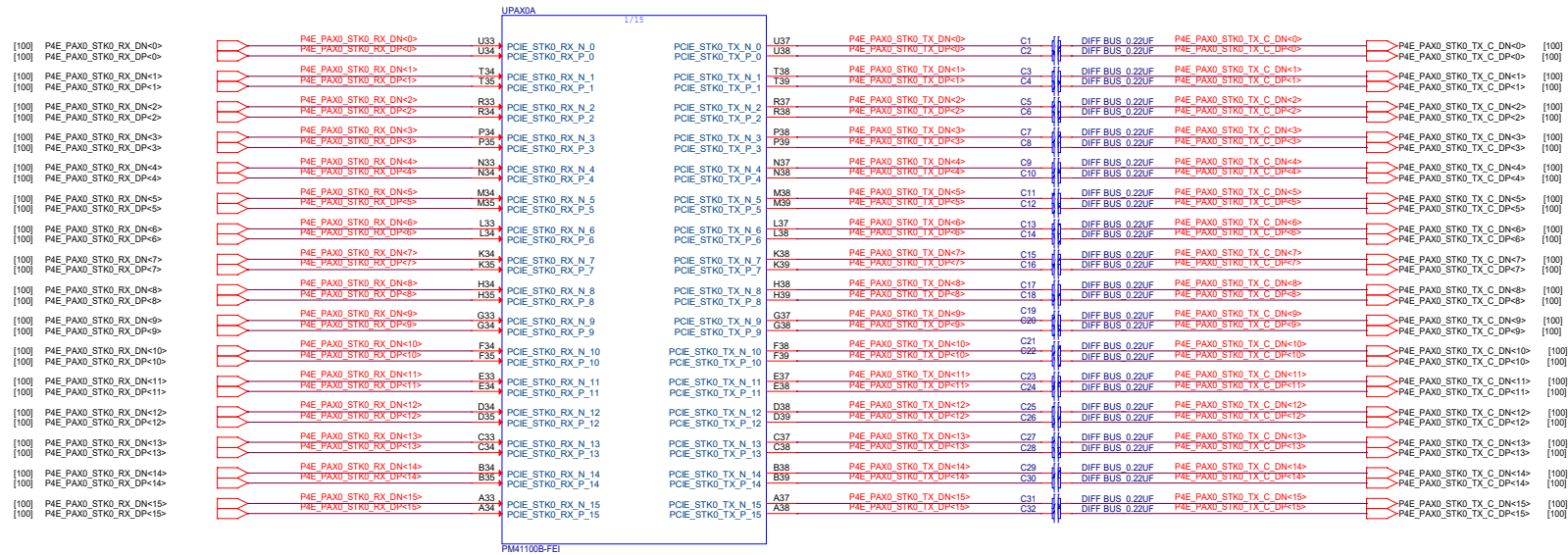
Note:

Bootstrap pins can be used as functional GPIOs or other modes after the switch has booted. The pins only need to retain these values during FW boot. After this point, these pins can be used for other purposes.

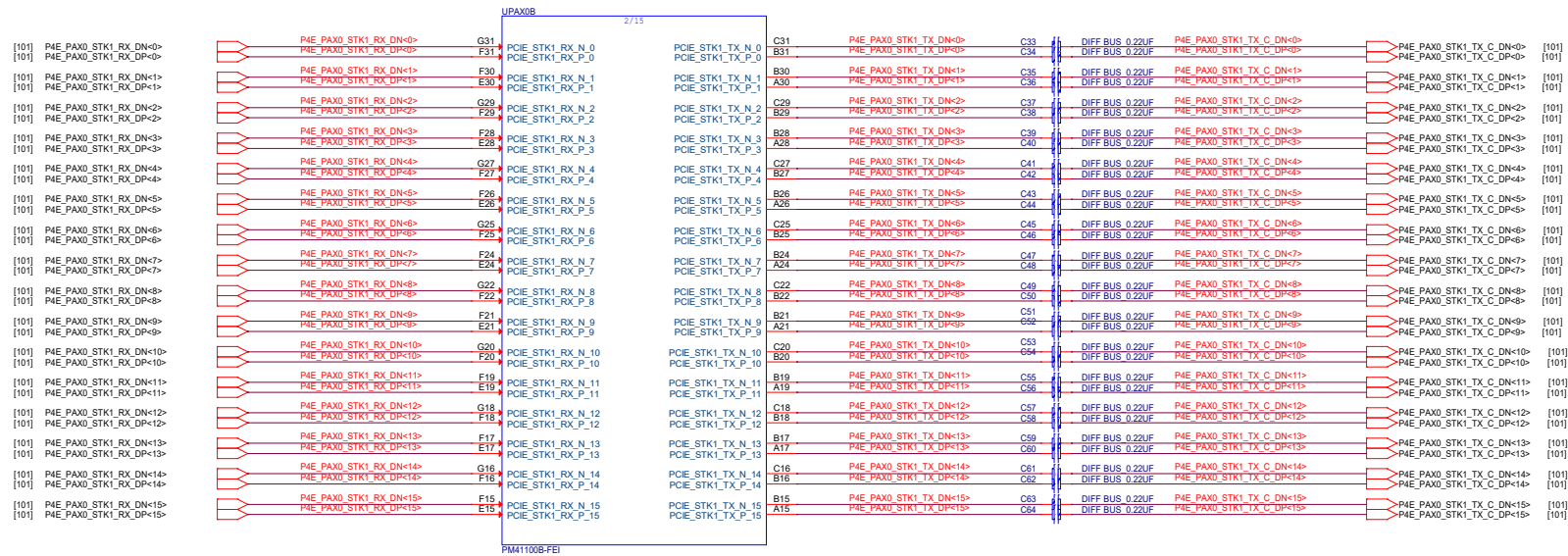
Table 494 • Bootstrap Pin Descriptions

Signal Name	Pin Name	Type	Function
BOOTSTRAP[0]	GPIO[96]	1.8V CMOS Digital Input	Reserved 1b: For correct device operation
BOOTSTRAP[1]	GPIO[97]	1.8V CMOS Digital Input	Inline ECC 0b: Inline ECC is disabled 1b: Inline ECC is enabled
BOOTSTRAP[2]	GPIO[98]	1.8V CMOS Digital Input	Reserved 0000b: For correct device operation
BOOTSTRAP[3]	GPIO[99]		
BOOTSTRAP[4]	GPIO[100]		
BOOTSTRAP[5]	GPIO[101]		
BOOTSTRAP[6]	GPIO[102]		
BOOTSTRAP[7]	GPIO[103]		
BOOTSTRAP[8]	GPIO[104]	1.8V CMOS Digital Input	SPI Addressing Mode 0b: Use 3B Addressing (<= 16 MB Flash) 1b: Use 4B Addressing (> 16 MB Flash) Note: Use 3B mode when addressing a SPI flash with image size <= 8MB if ECC is enabled. Use 4B mode when addressing a SPI flash with image size > 8 MB if ECC is enabled.

BOOTSTRAP[9]	GPIO[105]	1.8V CMOS Digital Input	Reserved 0b: For correct device operation, but provides an option to connect a pull-up for future use-cases.
BOOTSTRAP[10]	GPIO[106]	1.8V CMOS Digital Input	Reserved 1b: For correct device operation, but provides an option to connect a pull-down for future use-cases.
BOOTSTRAP[11]	GPIO[84]	1.8V CMOS Digital Input	Reserved 1b: For correct device operation, but provides an option to connect a pull-down for future use-cases.
BOOTSTRAP[12]	GPIO[85]	1.8V CMOS Digital Input	TWI_RECOVERY Address bit 0 This bootstrap controls the first bit of the lower 2 bits of the TWI address used for BL1 disaster recovery. The remaining bits are programmed in the one-time-programmable memory registers. The default Boot Recovery TWI address is 0x58 if these bits are set to 00b and the one-time-programmable (OTP) register is left at default.
BOOTSTRAP[13]	GPIO[86]	1.8V CMOS Digital Input	TWI_RECOVERY Address bit 1 This bootstrap controls the second bit of the lower 2 bits of the TWI address used for BL1 disaster recovery. The remaining bits are programmed in the one-time-programmable memory registers. The default Boot Recovery TWI address is 0x58 if these bits are set to 00b and the one-time-programmable (OTP) register is left at default.
BOOTSTRAP[14]	GPIO[87]	1.8V CMOS Digital Input	Secure Boot Dry Run Mode Select This bootstrap controls a dry run mode in the switch which enables secure boot validation without permanently setting the switch security state in one-time-programmable (OTP) memory. Enabling this mode will cause the switch to operate as if the security state of the switch is set to <i>initialized secure</i> . 0b: Disable dry-run mode: Switchtec will follow the security state from OTP memory 1b: Enable dry-run mode: Switchtec will treat the switch as <i>initialized secure</i> and validate images Note: Enabling dry-run mode when the security mode in OTP is set to <i>initialized secure</i> has no effect on the switch. The device will operate in secure mode as per the OTP setting.

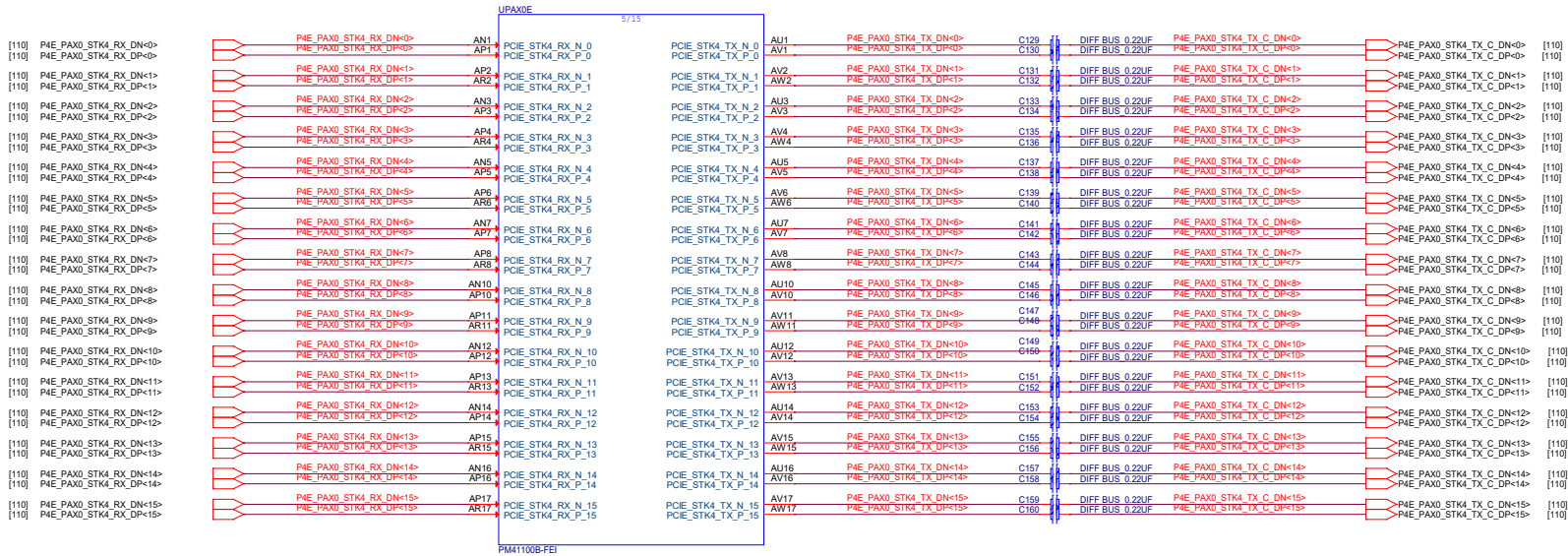


PAX0 STK0 to Whisper Downstream

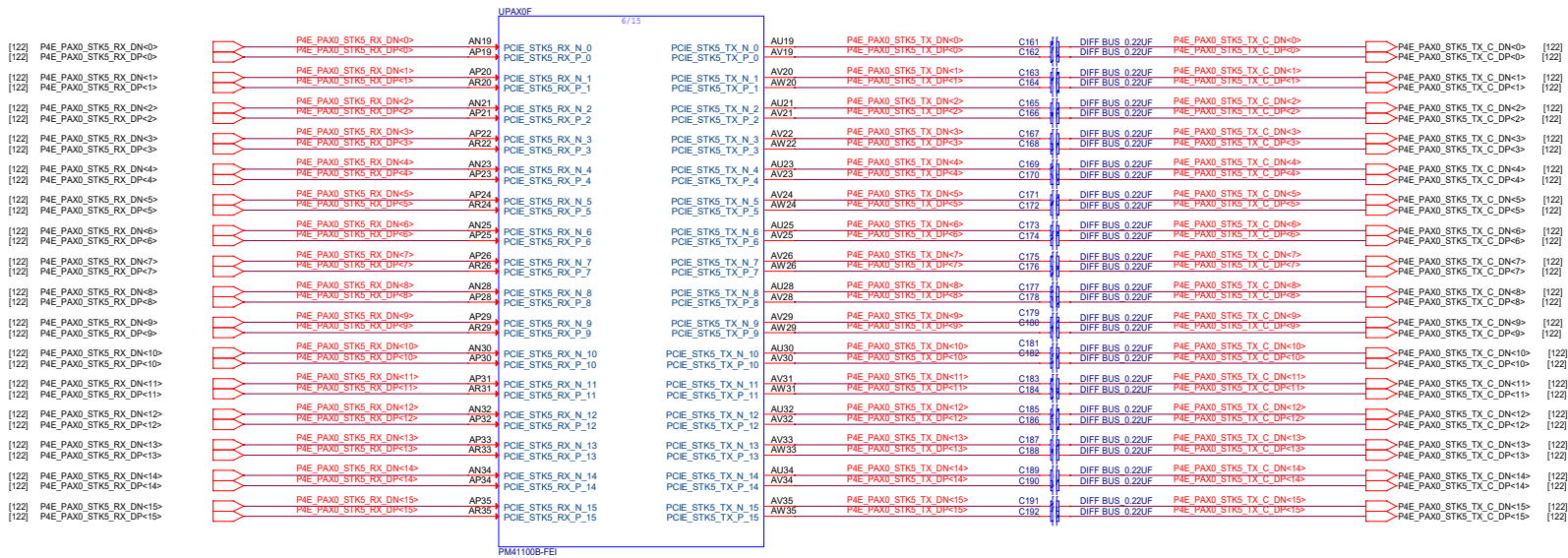


PAX0 STK1 to Whisper Downstream

PAX0_STATION_0_1



PAX0 STK4 to OCP0

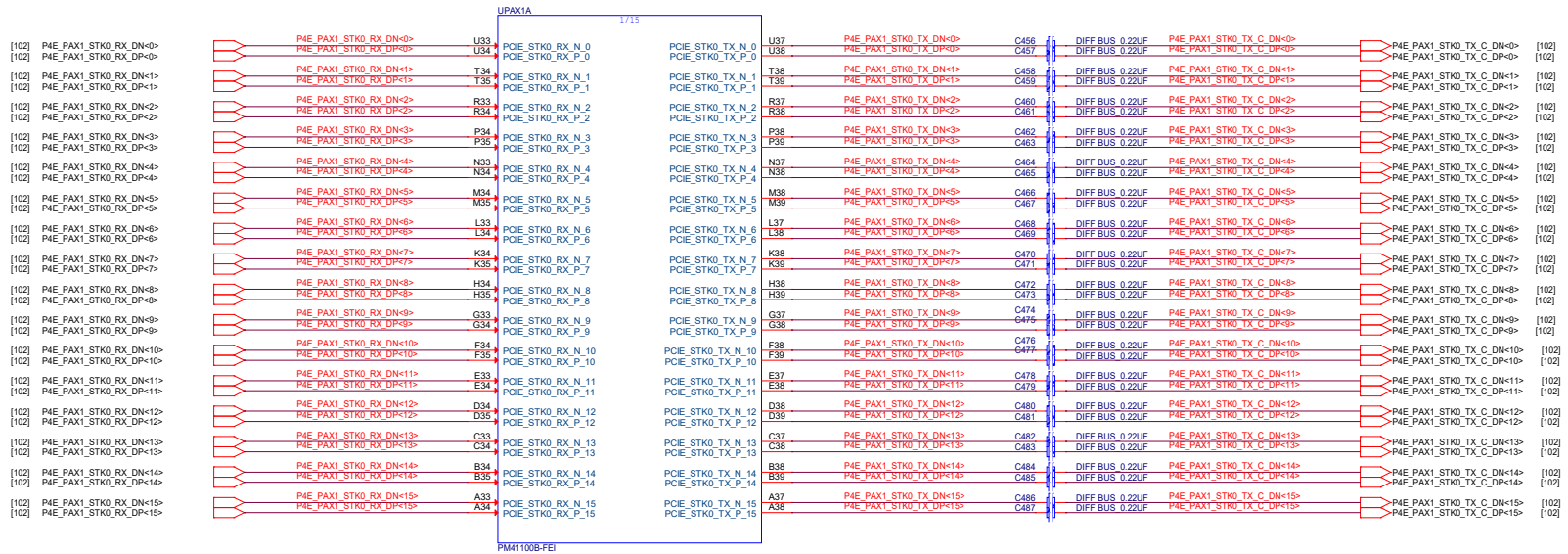


PAX0 STK5 to OCP4

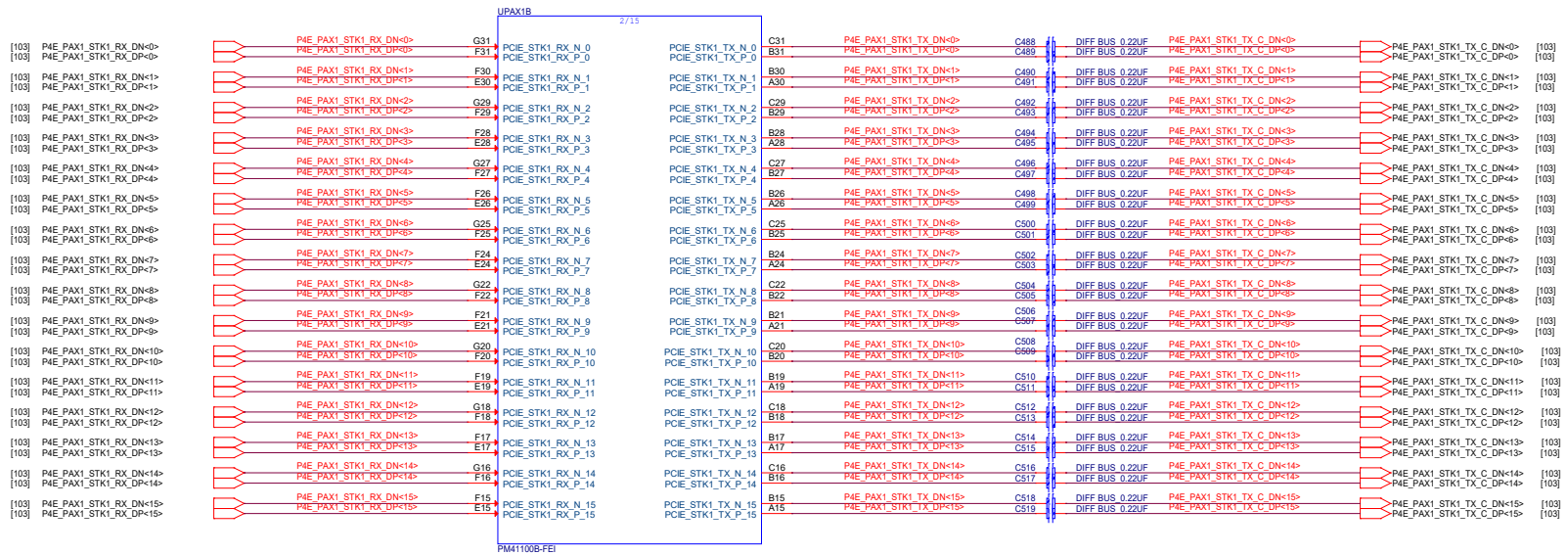






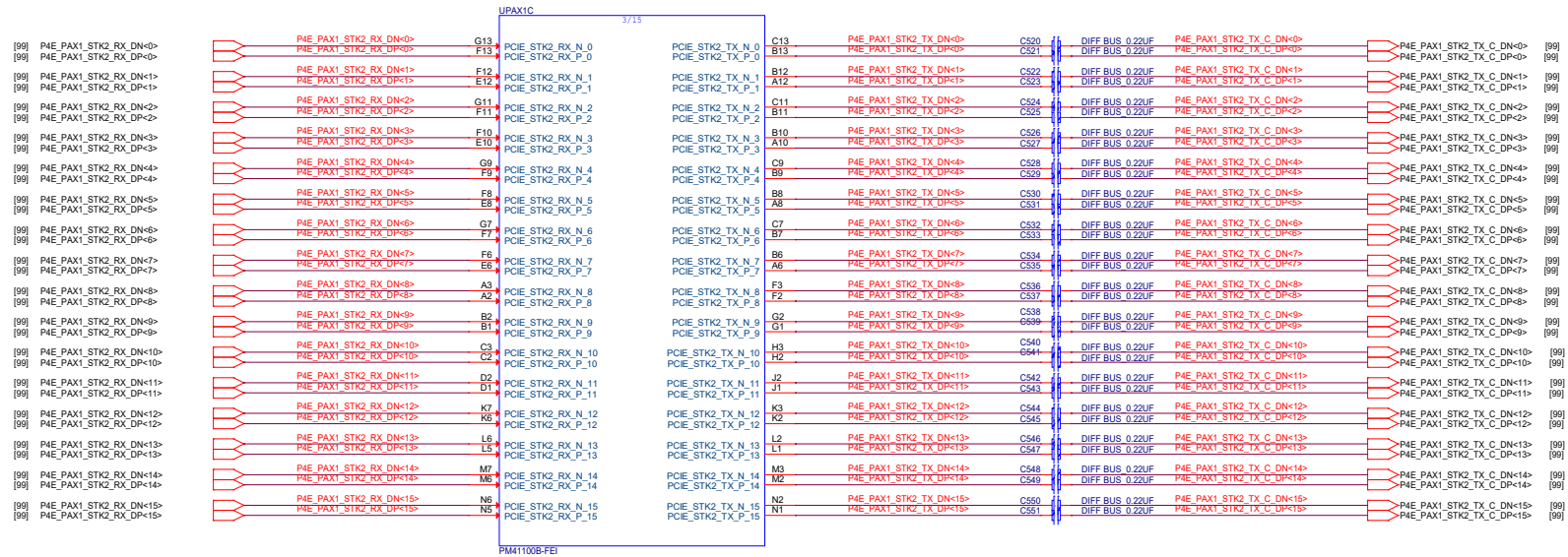


PAX1 STK0 to Whisper Downstream

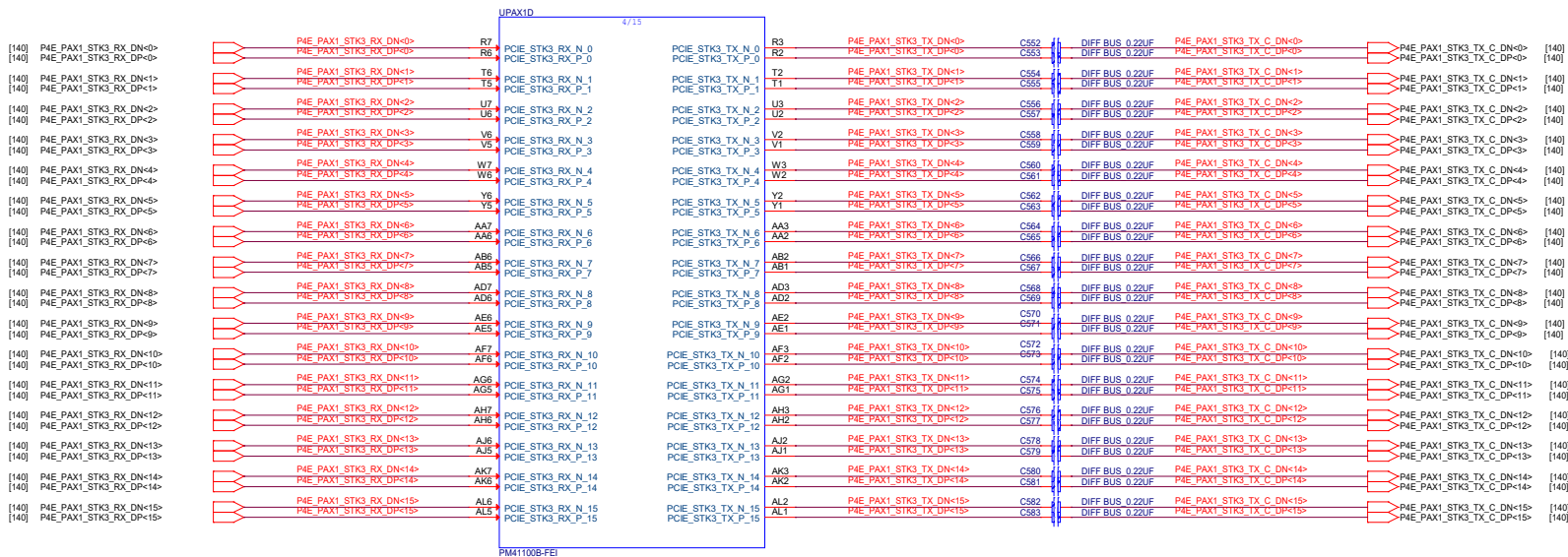


PAX1 STK1 to Whisper Downstream

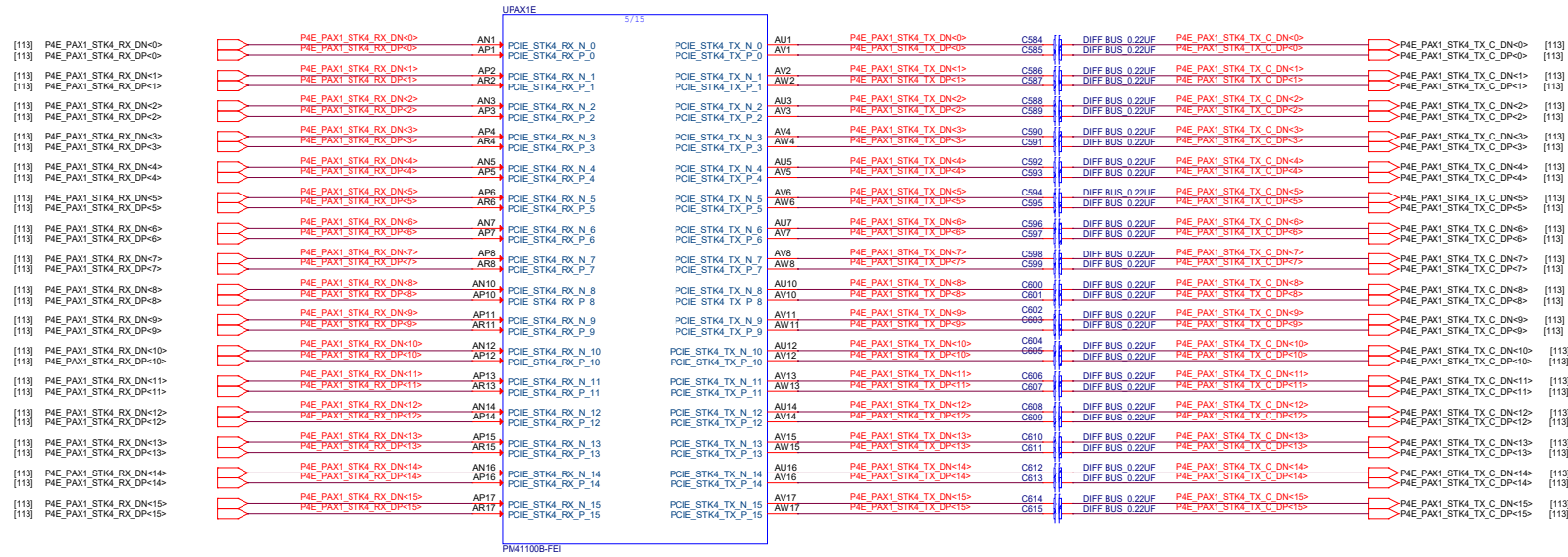
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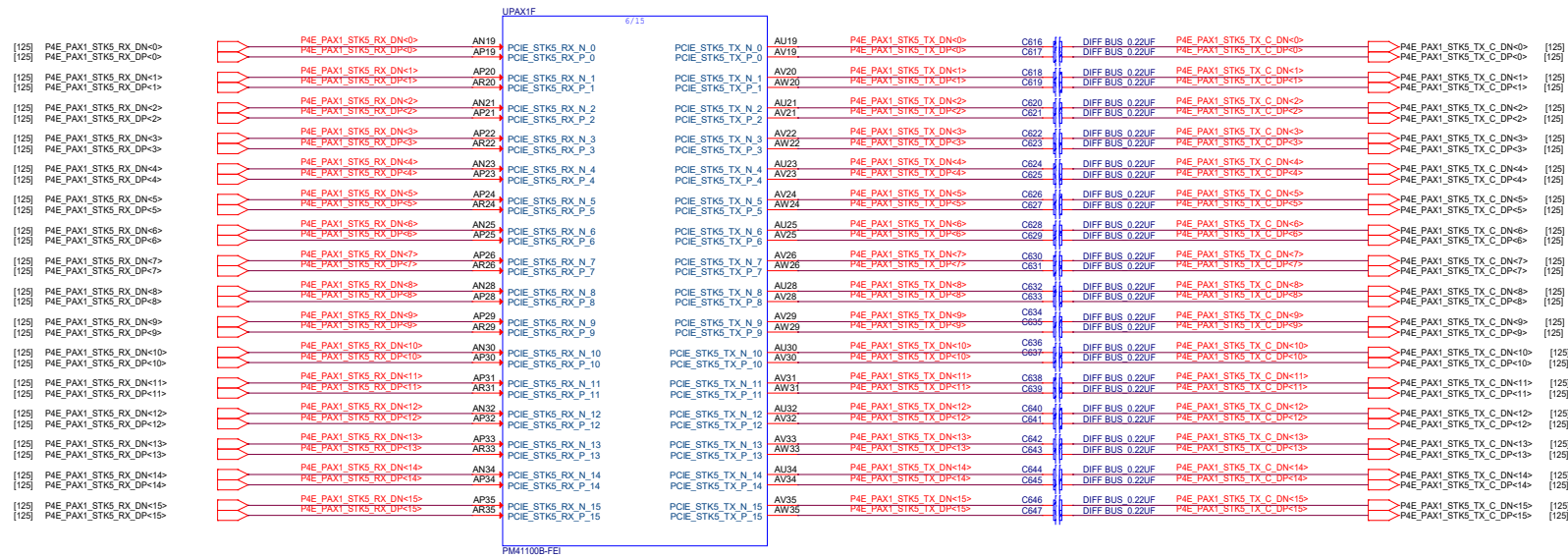
PAX1 STK2 to Whisper Upstream



PAX1 STK3 to NVMe1



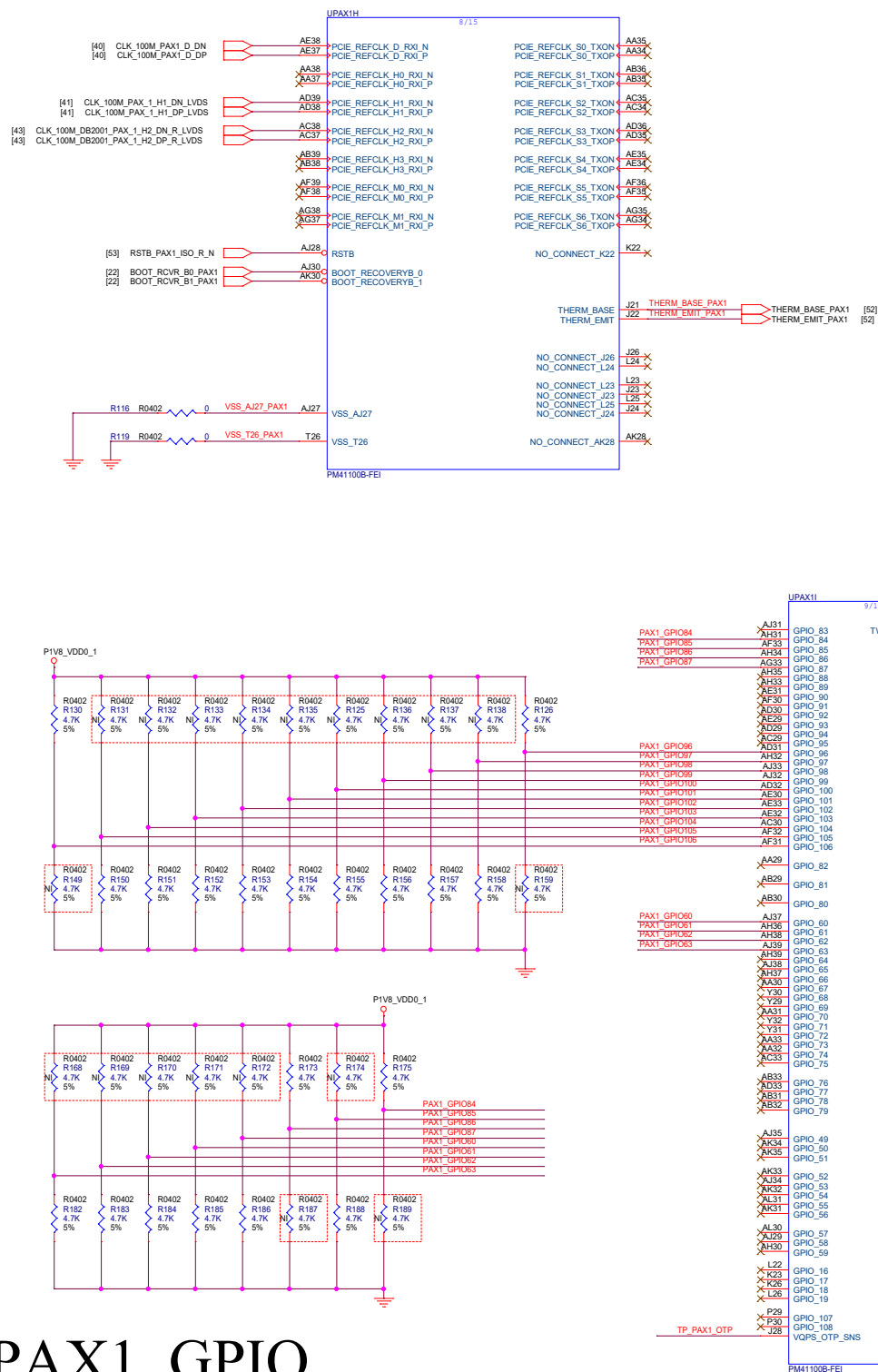
PAX1 STK4 to OCP1



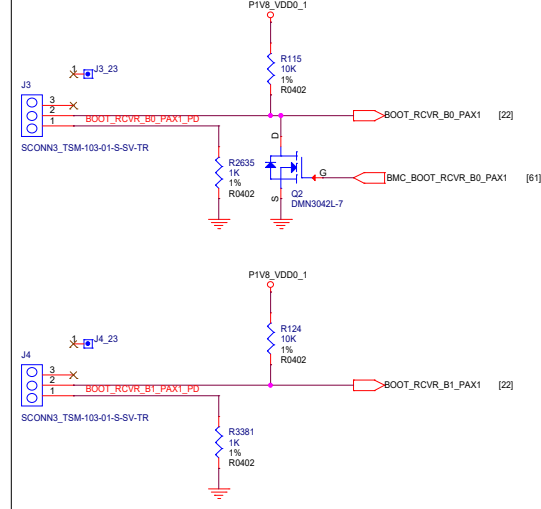
PAX1 STK5 to OCP5

PAX1_STATION_4_5

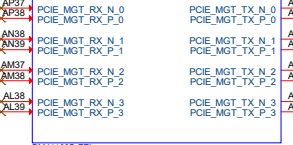
PAX1_GPIO



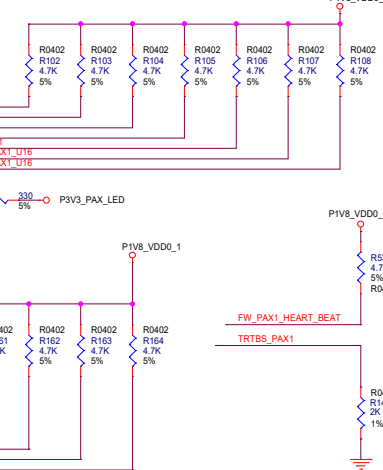
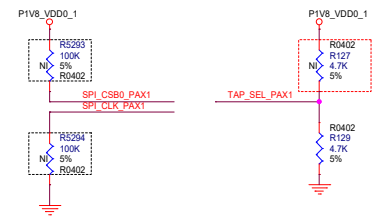
Boot Recovery Mode Jumper



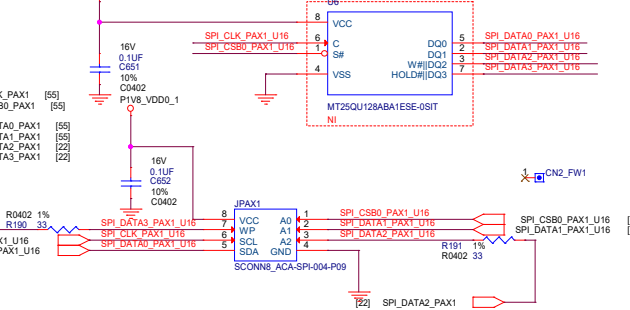
UPAX1G



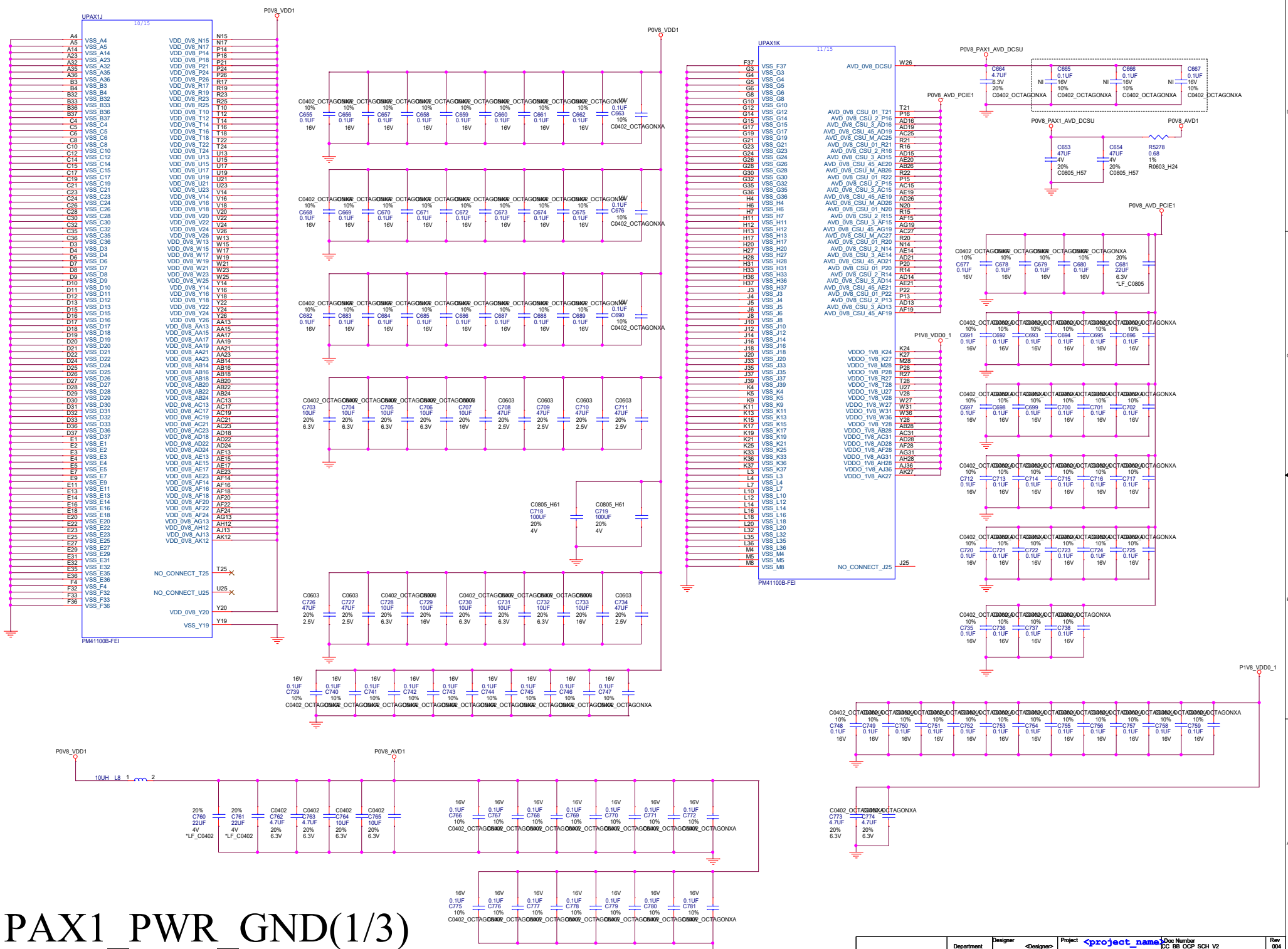
PAX1_SYNC
PAX1_ALERT_N
SMB_PAX1_TWI0_R_SDA
PAX1_TWI_SRSTB_RCVRY

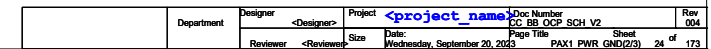


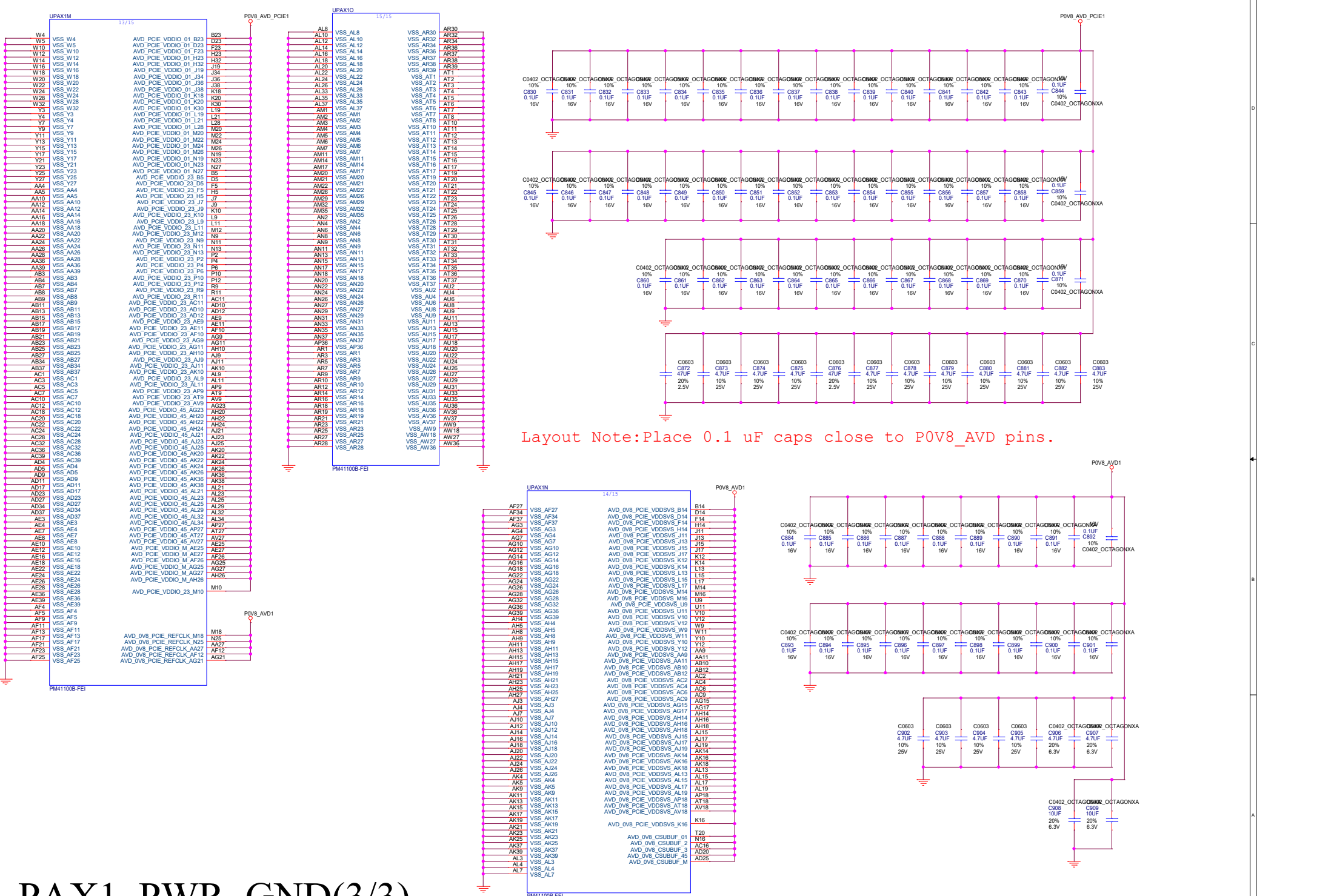
CO-LAYOUT



PAX1_PWR_GND(1/3)

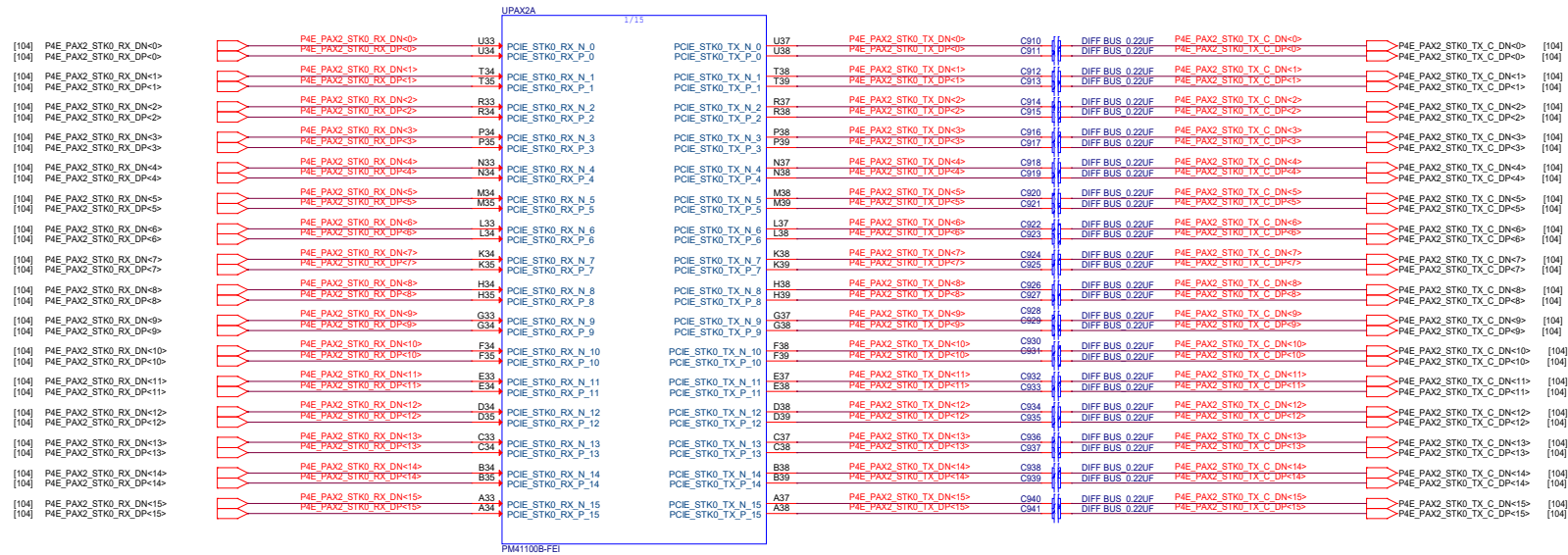




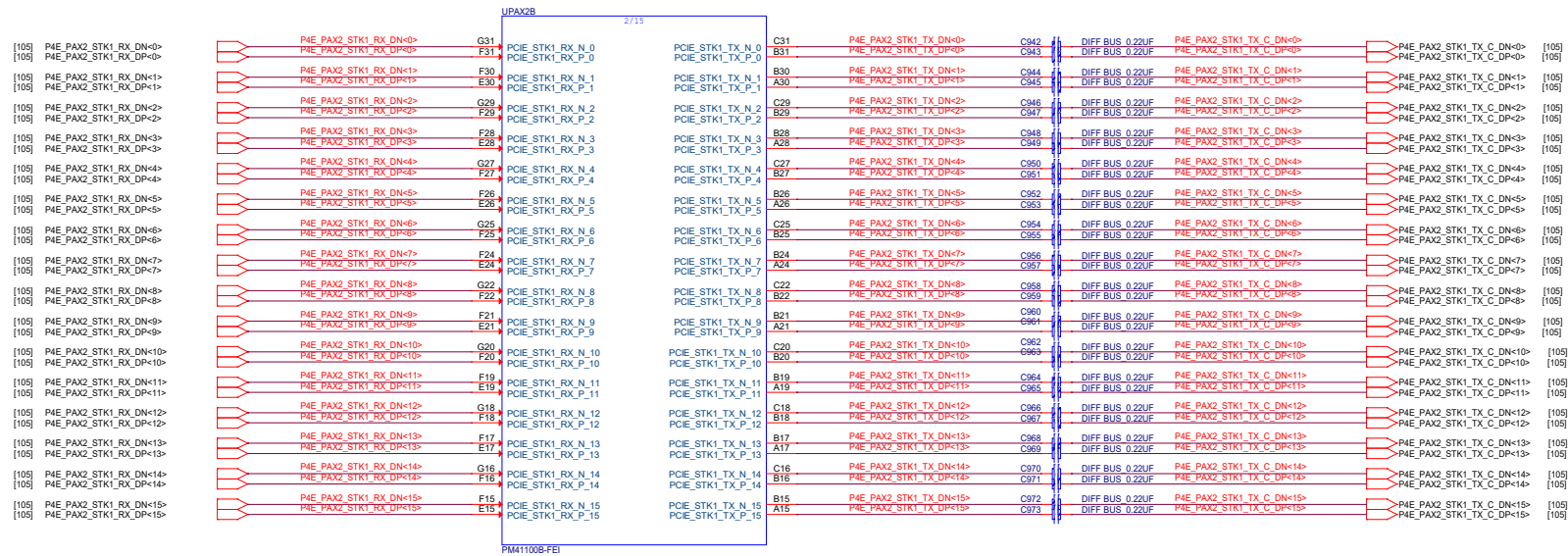


PAX1_PWR_GND(3/3)

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Reviewer	<Reviewer>	Date:	Page Title	Sheet
		Wednesday, September 20, 2023	PAX1_PWR_GND(3/3)	25 of 173

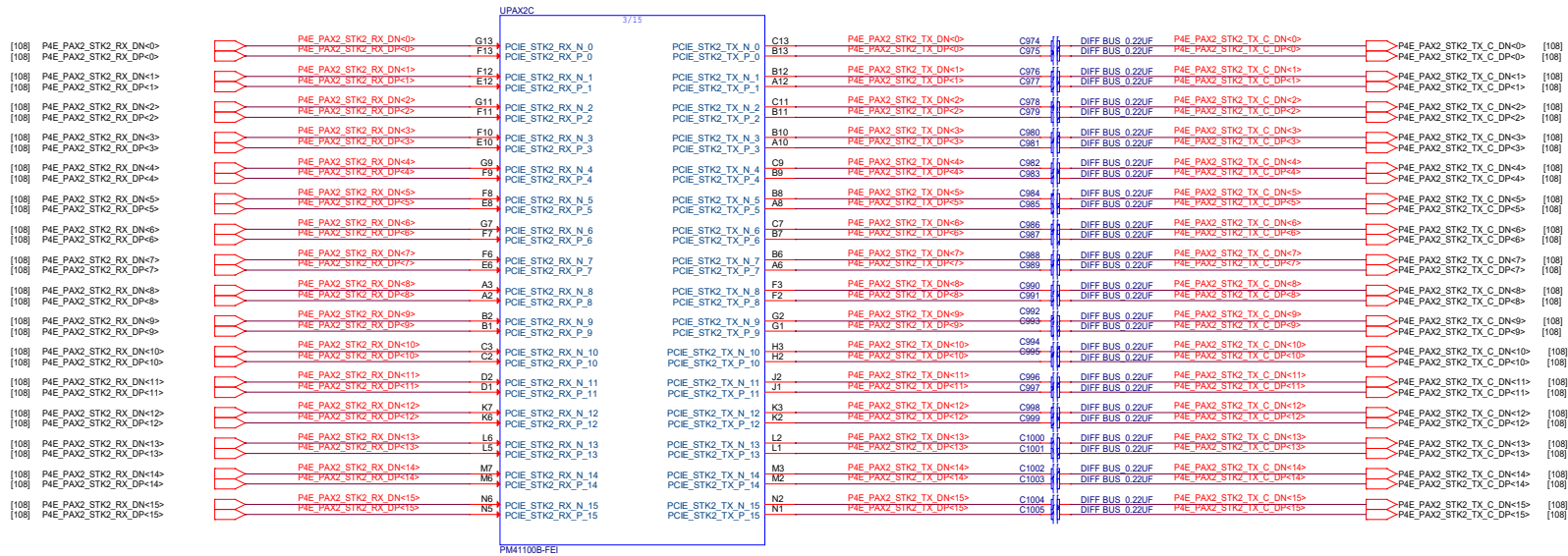


PAX2 STK0 to Whisper Downstream

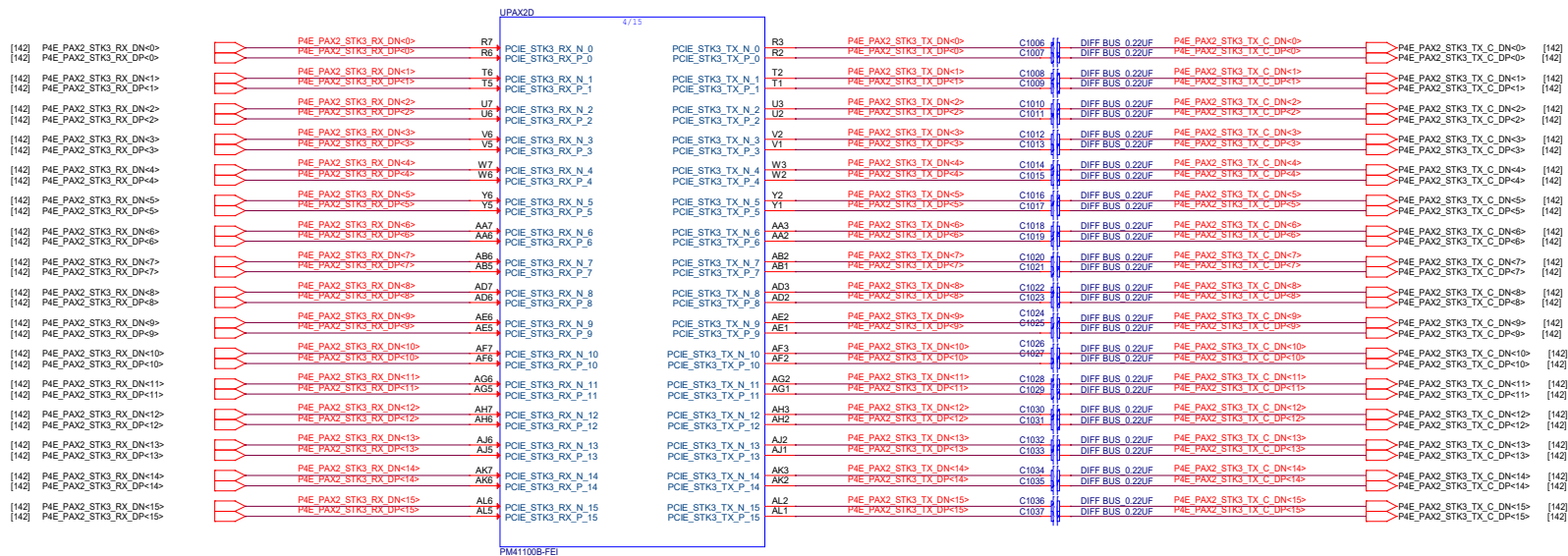


PAX2 STK1 to Whisper Downstream

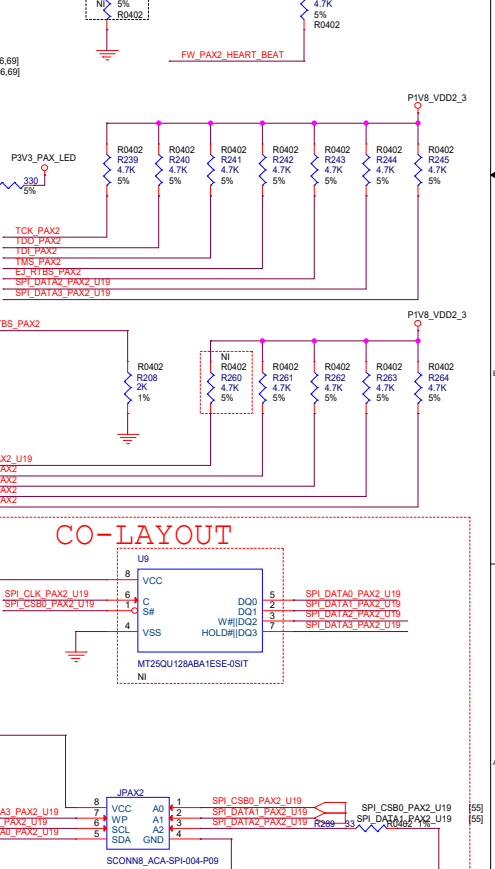
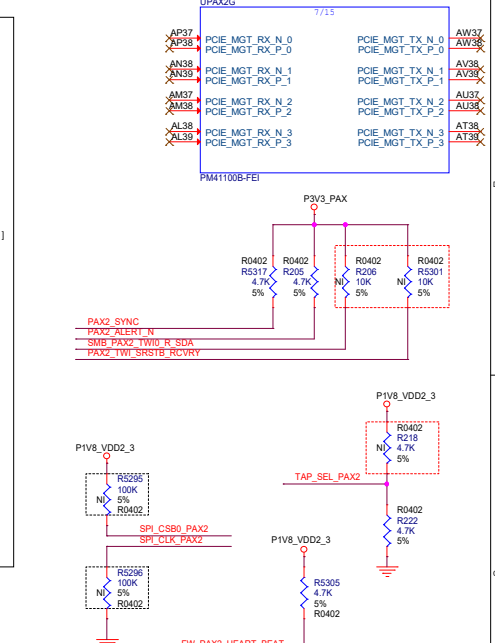
PAX2_STATION_0_1



PAX2 STK2 to Whisper Upstream



PAX2 STK3 to NVMe2

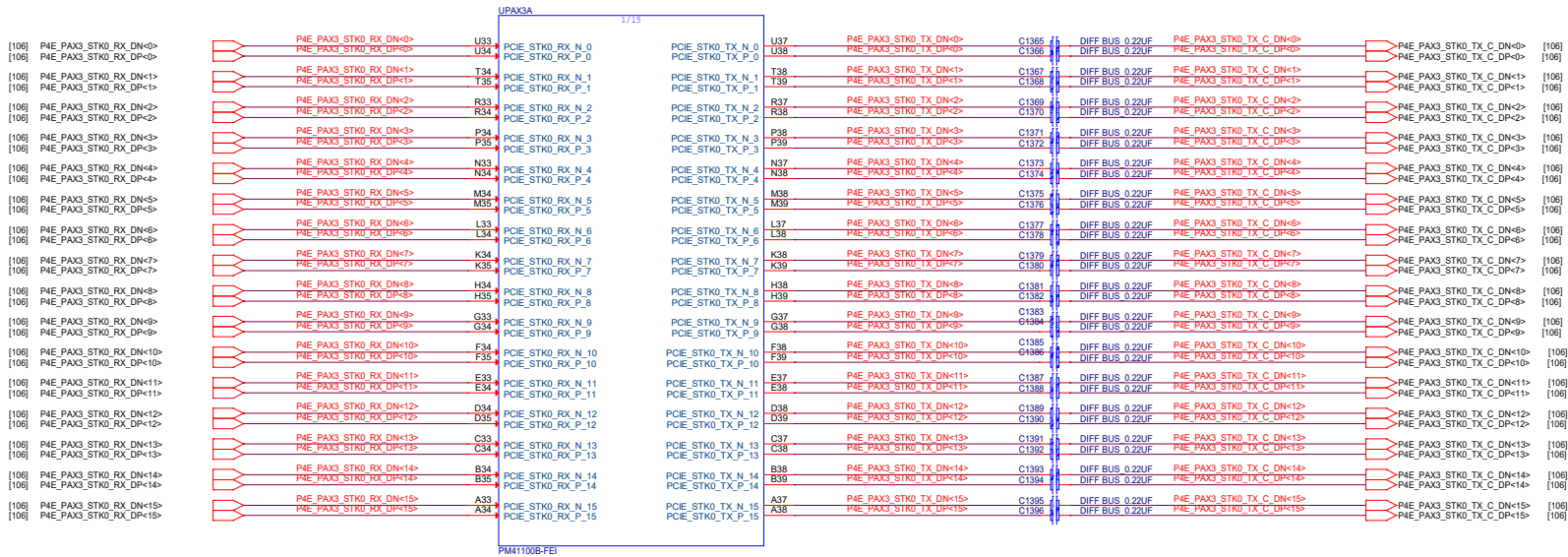


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		<Reviewer>		Wednesday, September 20, 2023	PAX2 GPIO
					Sheet 29 of 173

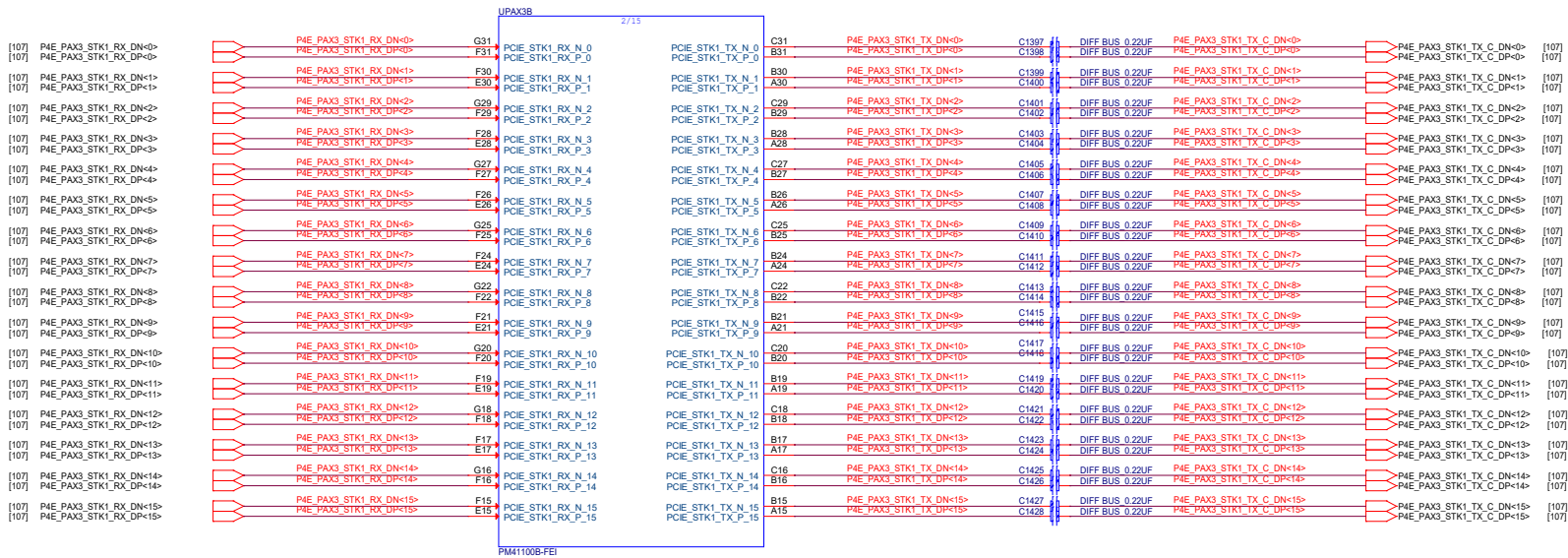






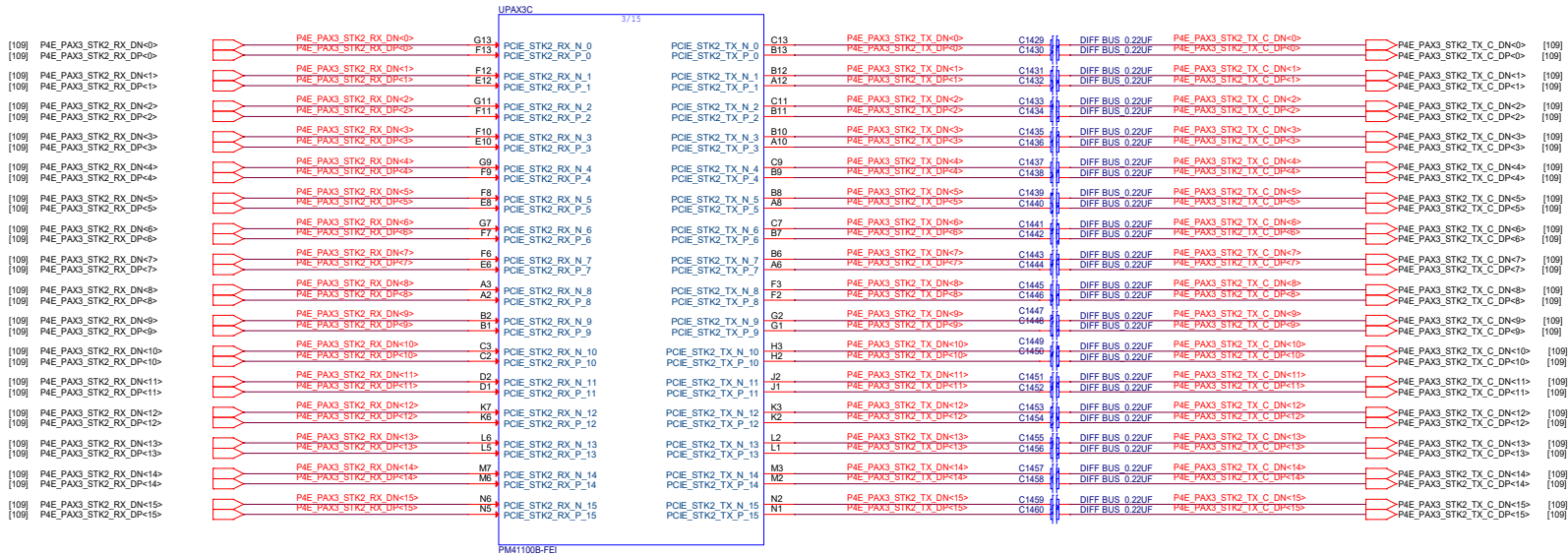


PAX3 STK0 to Whisper Downstream

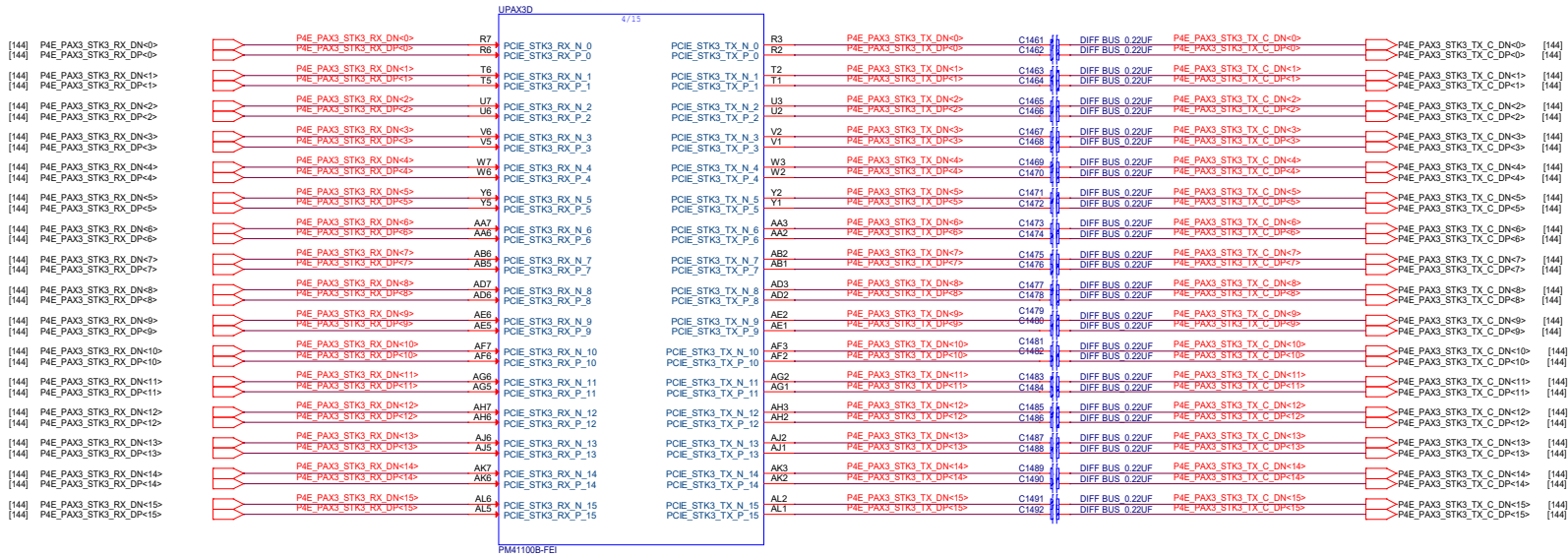


PAX3 STK1 to Whisper Downstream

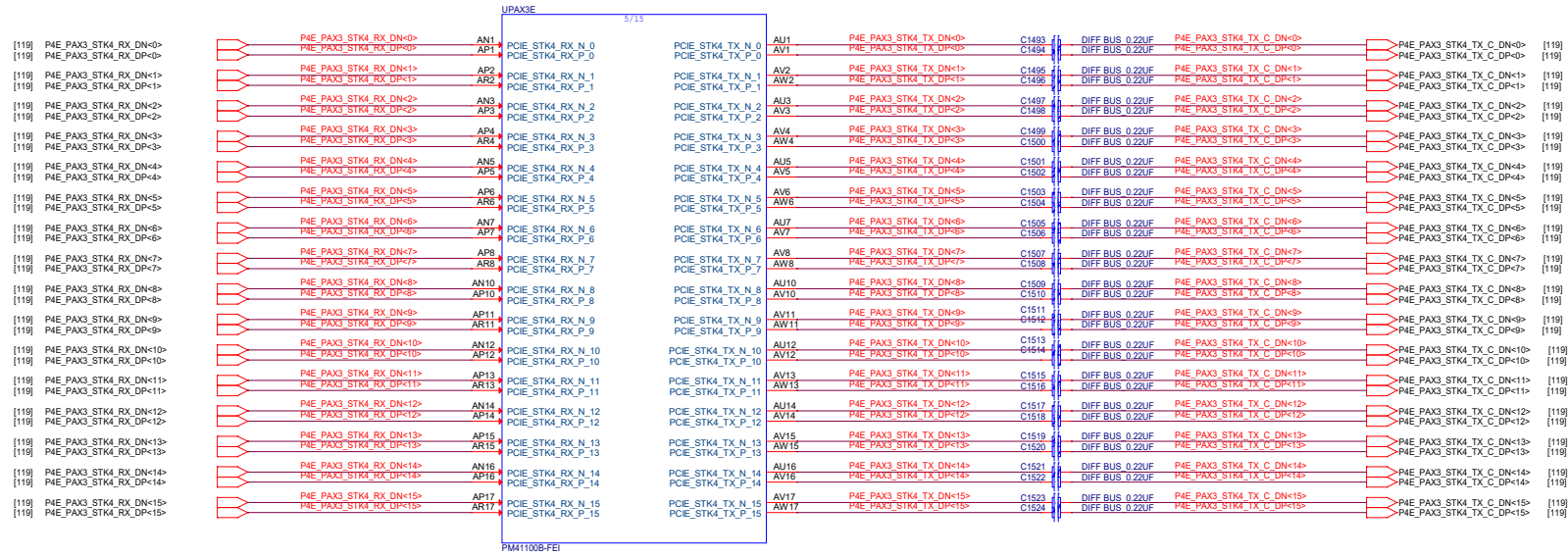
PAX3_STATION_0_1



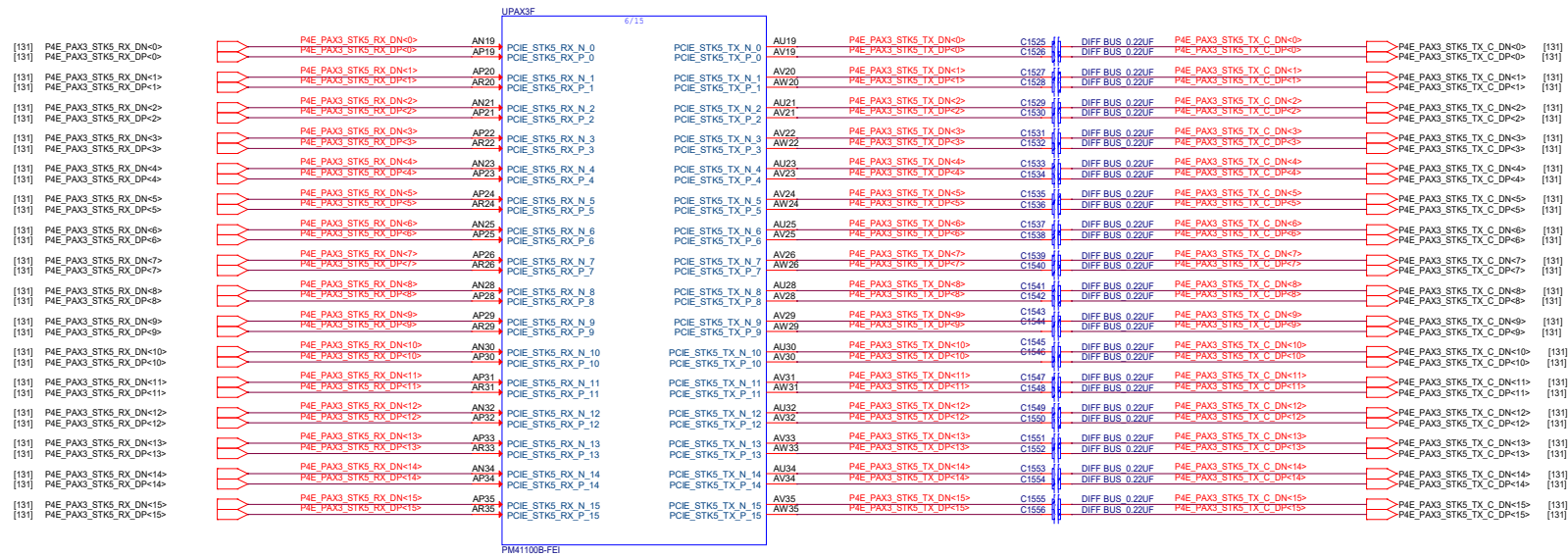
PAX3 STK2 to Whisper Upstream



PAX3 STK3 to NVMe3



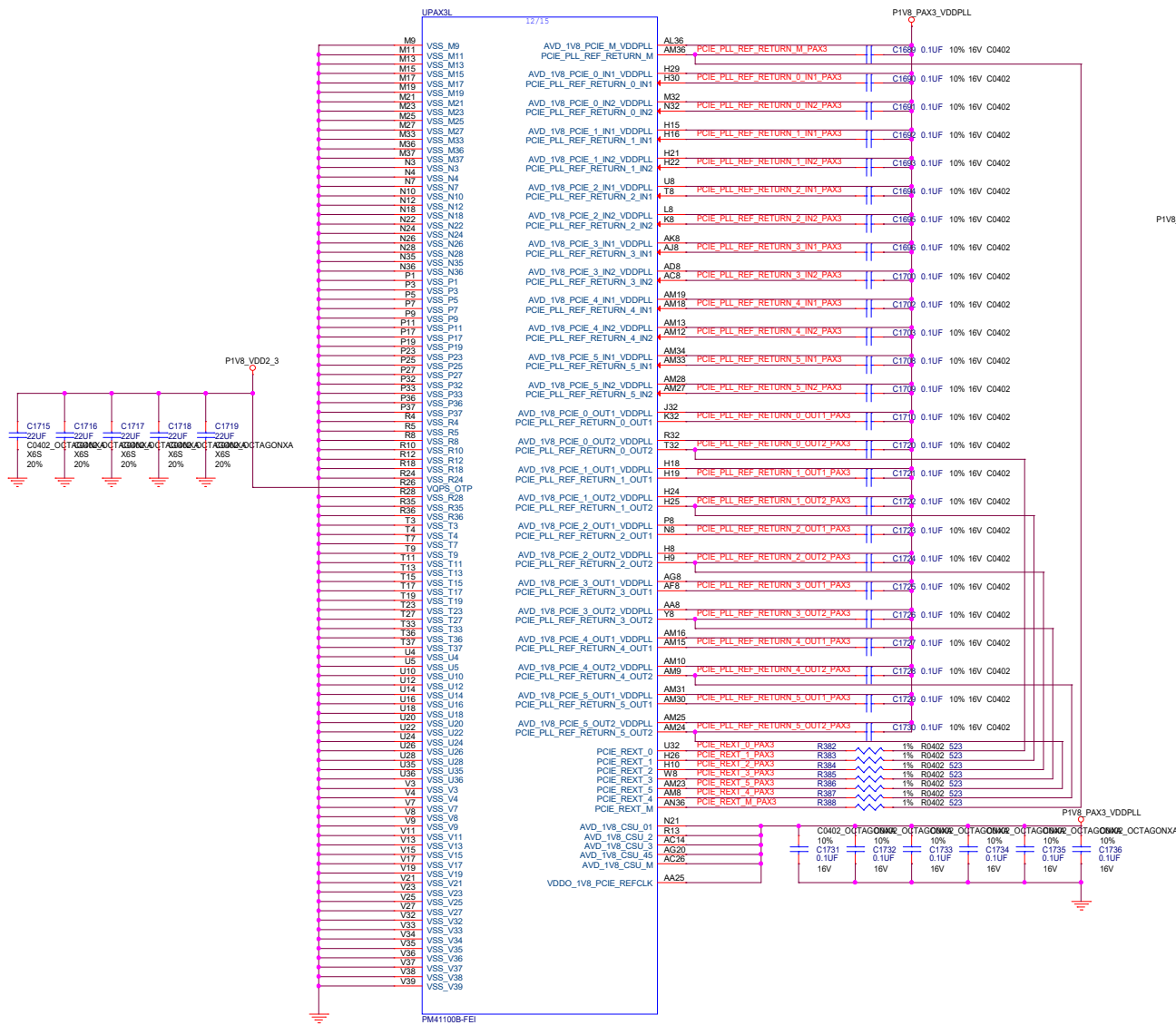
PAX3 STK4 to OCP3



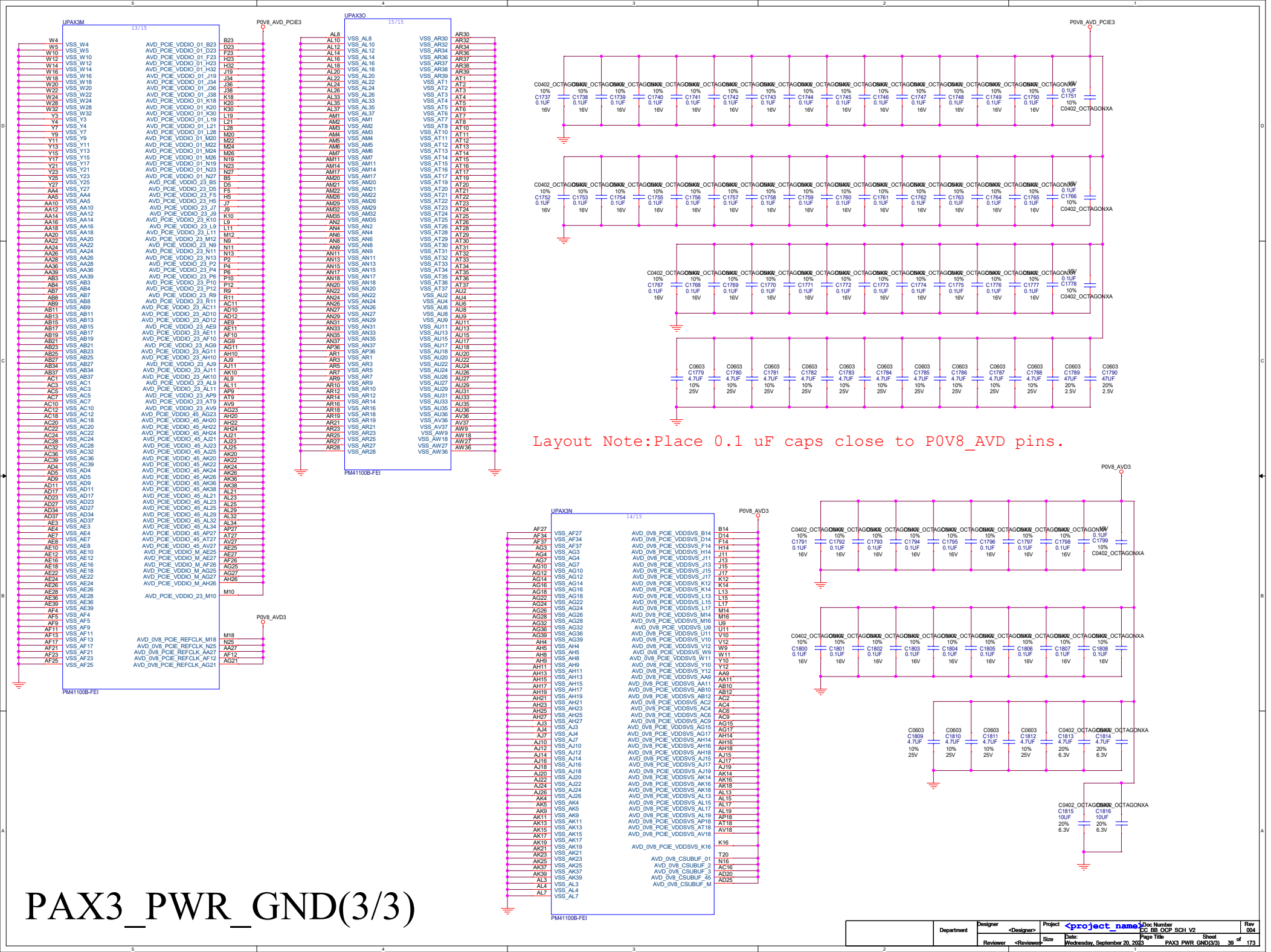
PAX3 STK5 to OCP7



PAX3_PWR_GND(2/3)

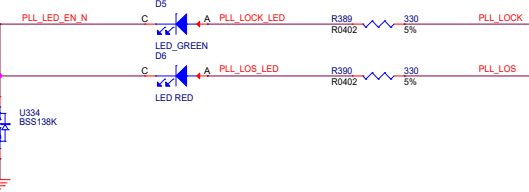


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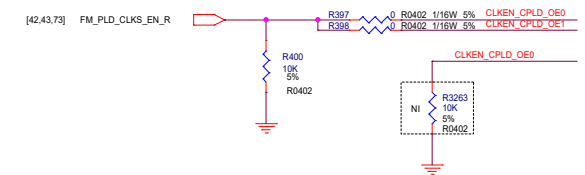
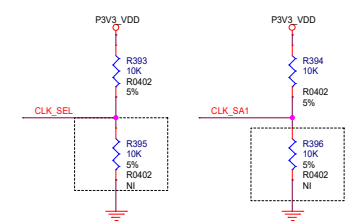
[42.43.51] SMB_BMC_ISO_SCL R2531 0 R0402 5% SMB_BMC_8T49N1012_SCL [40]
[42.43.51] SMB_BMC_ISO_SDA R2532 0 R0402 5% SMB_BMC_8T49N1012_SDA [40]

[69.72.75] LED_DBG_MODE_R



CAD NOTE: PLACE C1817 CLOSE TO PIN6,PIN65

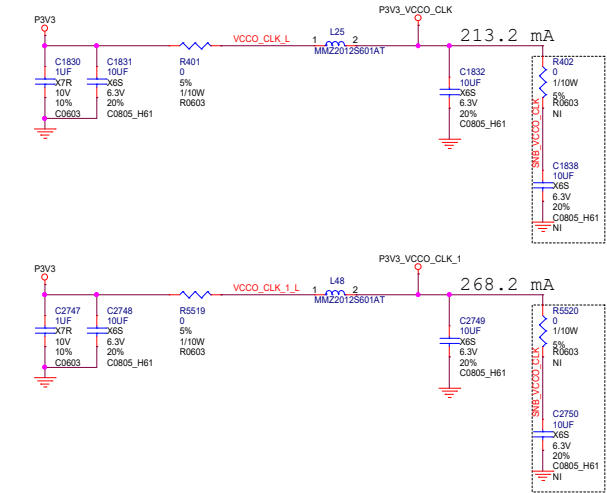
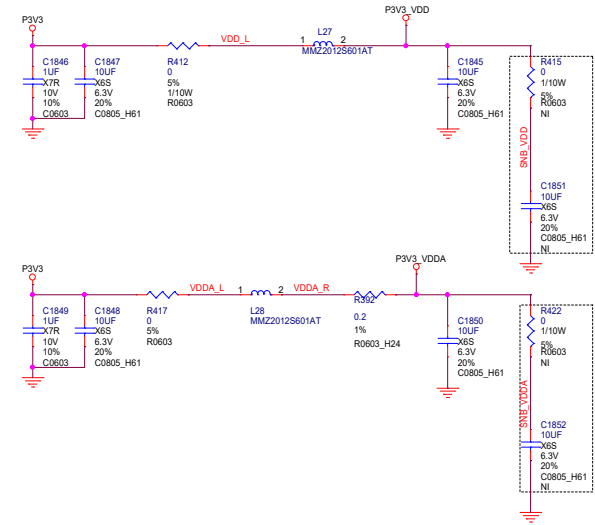
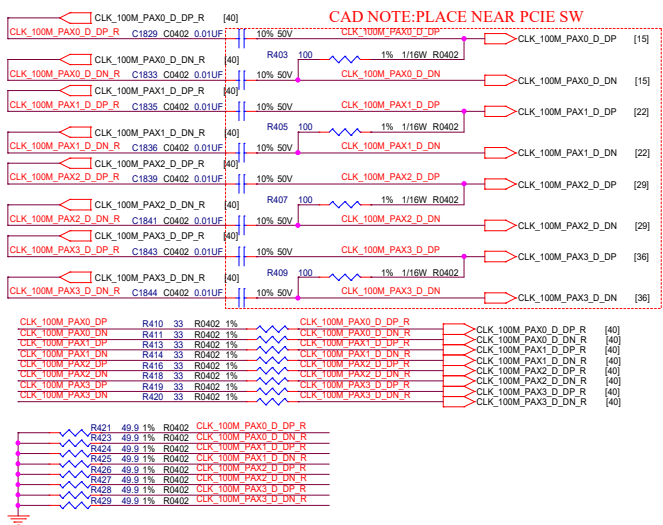
CLK_CAP C0402 X7R 16V C1817 0.1UF 10% CLK_CAP_REF
CLK_RST_R_N R0402 5% R391 10K P3V3_VDD



ADDRESS:0XDC

Output Impedance: 100 ohm

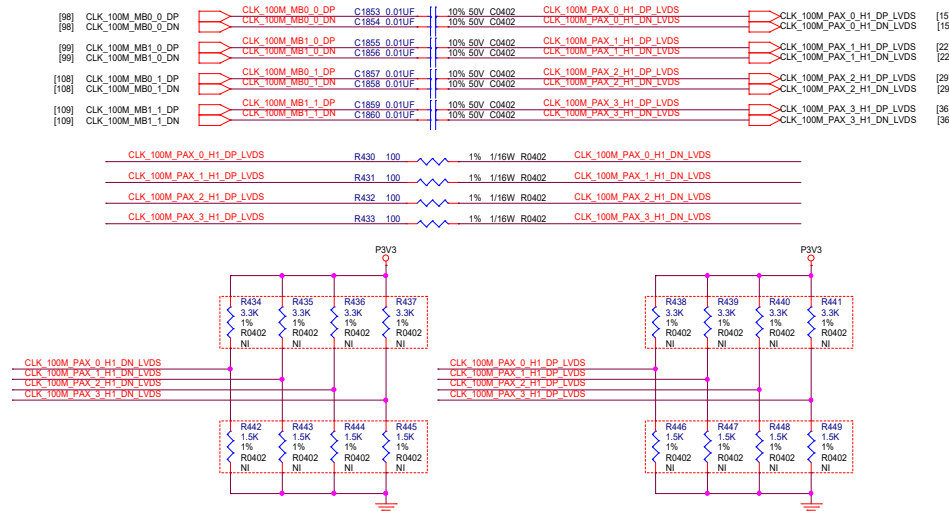
CAD NOTE: PLACE NEAR PCIE SW



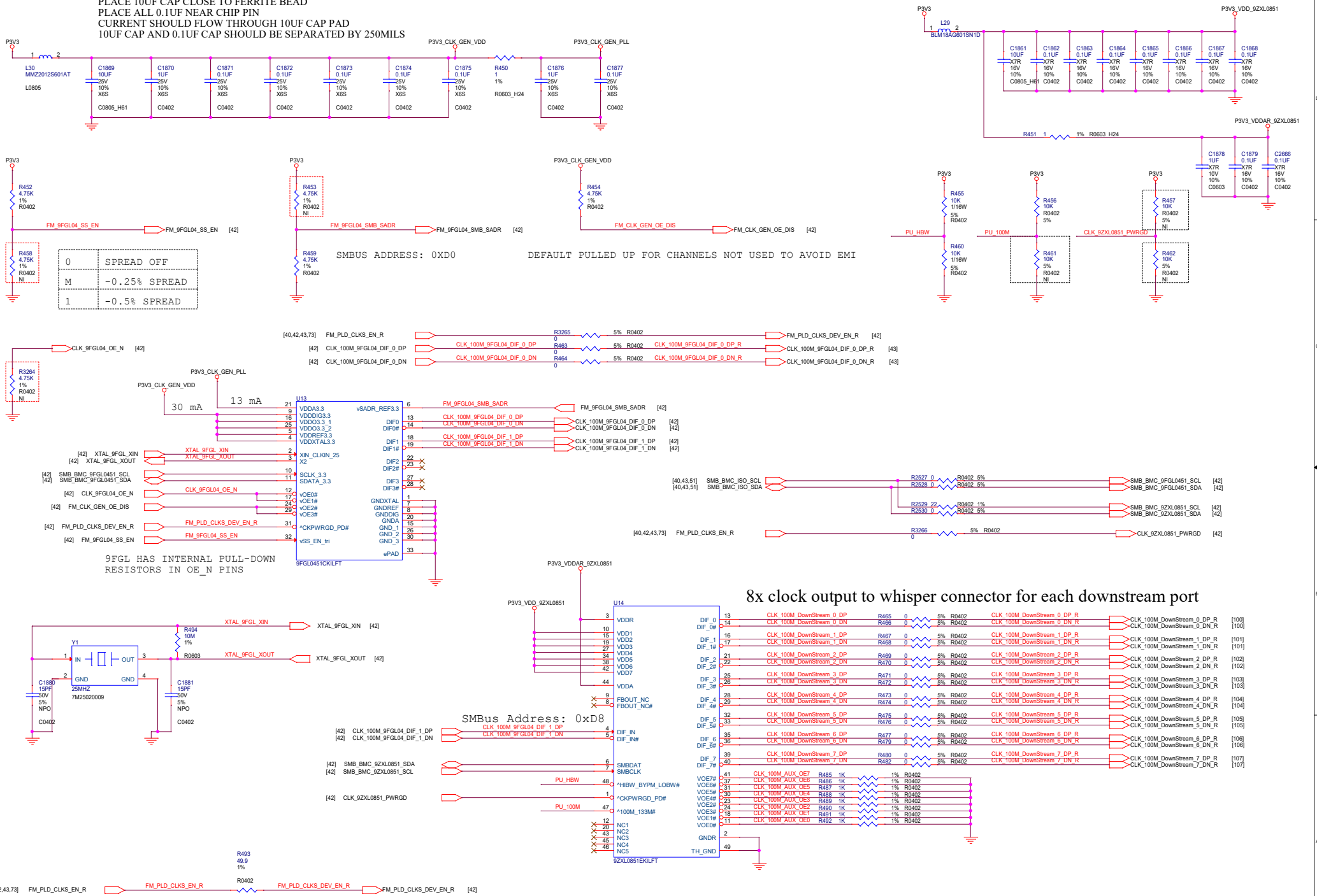
CLOCK GEN 100M 8T49N1012

LP-HCSL to LVDS

CAD NOTE:PLACE NEAR PCIE SW



CLOCK_COMMON

[illegible]

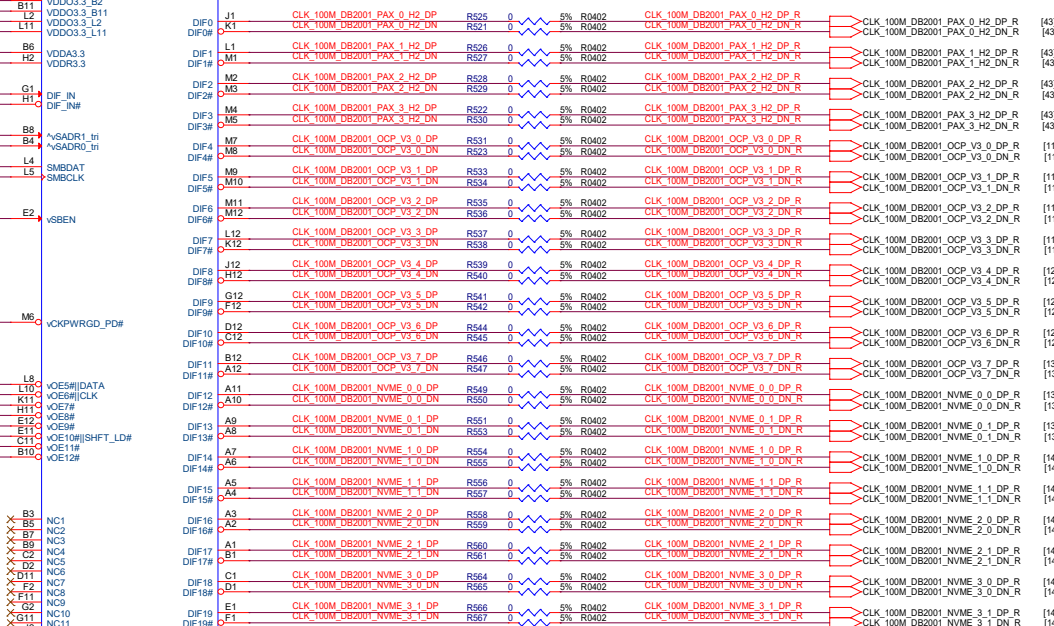
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		<Designer>	<project_name>	CC BB OCP SCH V2	004
		Reviewer	Size	Date	Page Title
1		<Reviewer>		Wednesday, September 20, 2023	CLOCK GEN 9FGL04 42 of 173

PLACE ALL 0.1UF CAP NEAR CHIP PIN

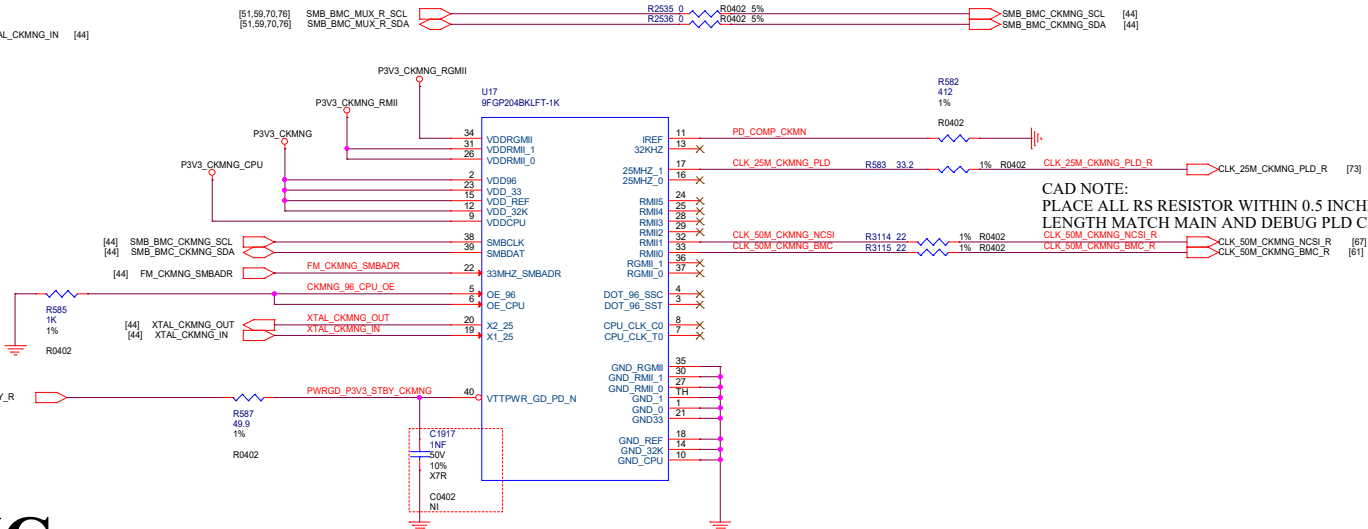
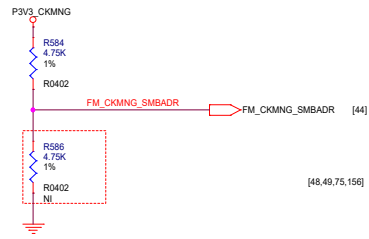
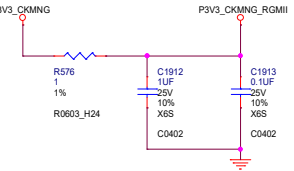
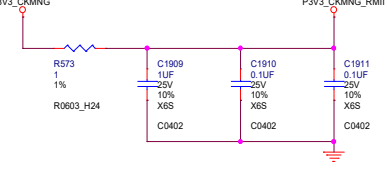
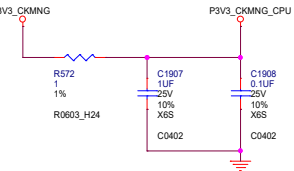


CAD NOTE:PLACE NEAR PCIE SW

CLK_100M_DB2001_PAX 0 H2_DP_R_LVDS	R500	100		1%	116W	R0402	CLK_100M_DB2001_PAX 0 H2_DN_R_LVDS
CLK_100M_DB2001_PAX 1 H2_DP_R_LVDS	R501	100		1%	116W	R0402	CLK_100M_DB2001_PAX 1 H2_DN_R_LVDS
CLK_100M_DB2001_PAX 2 H2_DP_R_LVDS	R502	100		1%	116W	R0402	CLK_100M_DB2001_PAX 2 H2_DN_R_LVDS
CLK_100M_DB2001_PAX 3 H2_DP_R_LVDS	R503	100		1%	116W	R0402	CLK_100M_DB2001_PAX 3 H2_DN_R_LVDS



	Department	Designer	Project	Doc Number	Rev
		<Designer>	<project_name>	CC_BB_OCP_SCH_V2	004
		Reviewer	Size	Date	Page Title
		<Reviewer>		Wednesday, September 20, 2023	Sheet CLK_BUFFER_DB2001 43 of 173

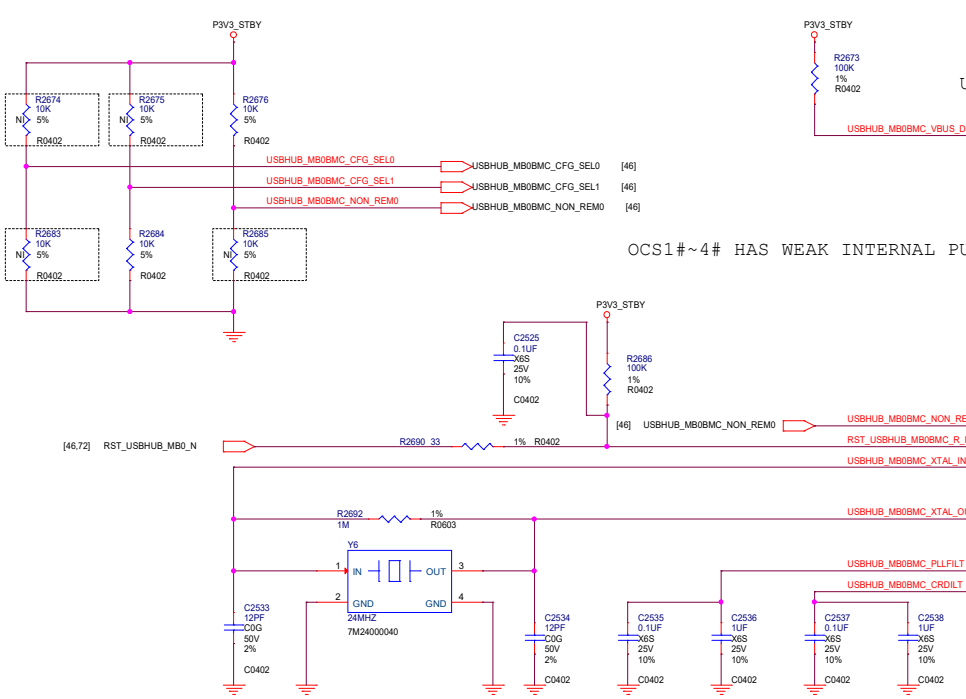
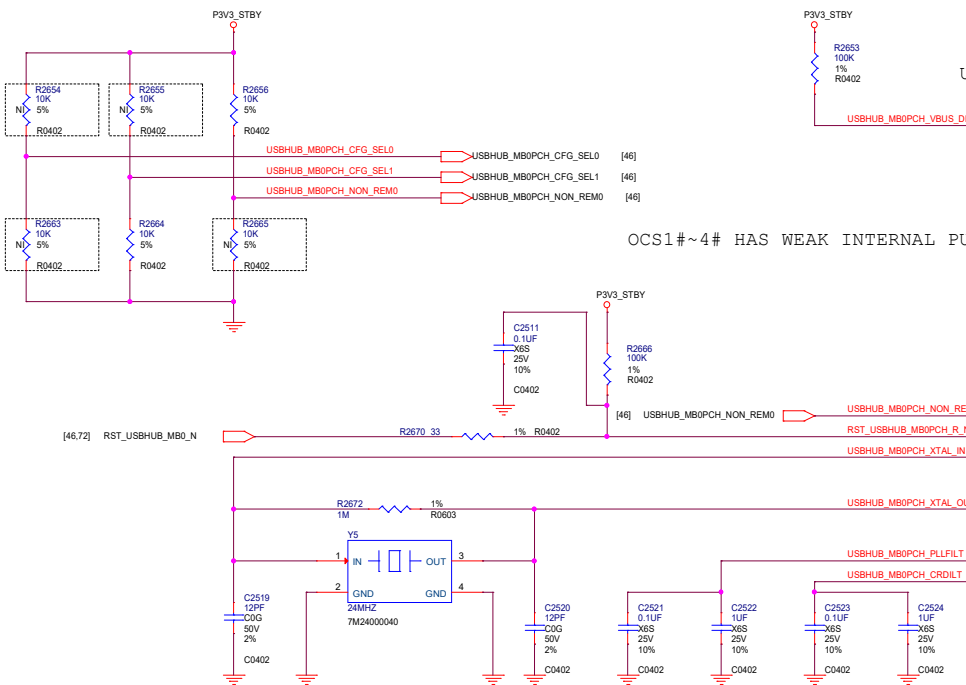
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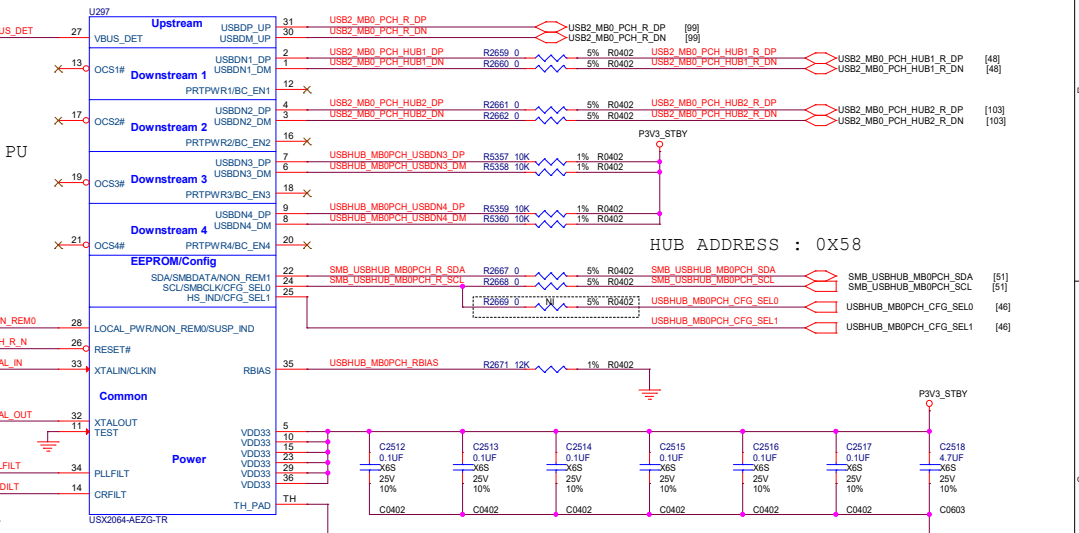
CLK_50M_CKMNG_NCSI_R      [67]
CLK_50M_CKMNG_BMC_R      [61]

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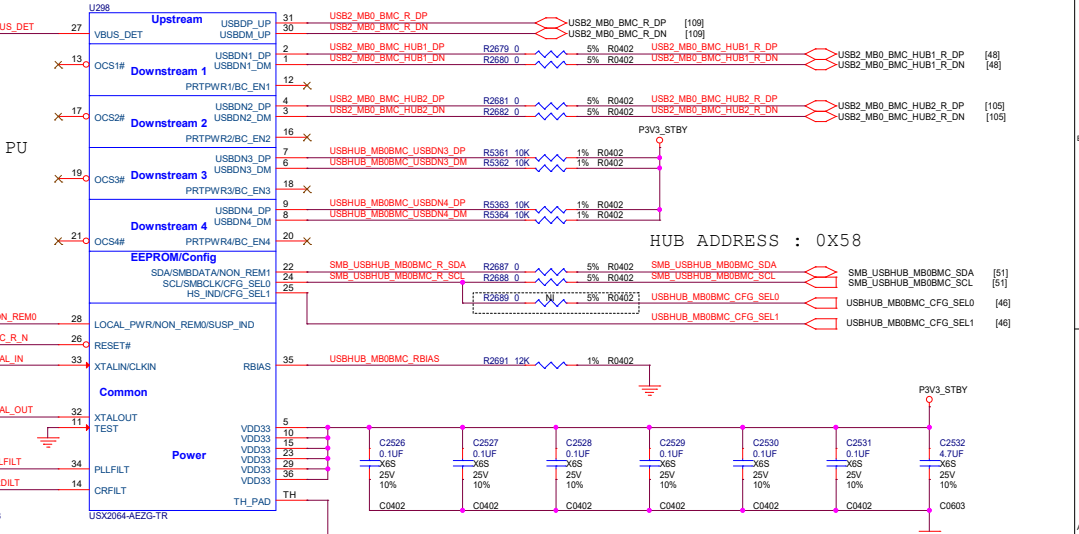
BLANK



USB 2.0 HUB FOR MB0 PCH



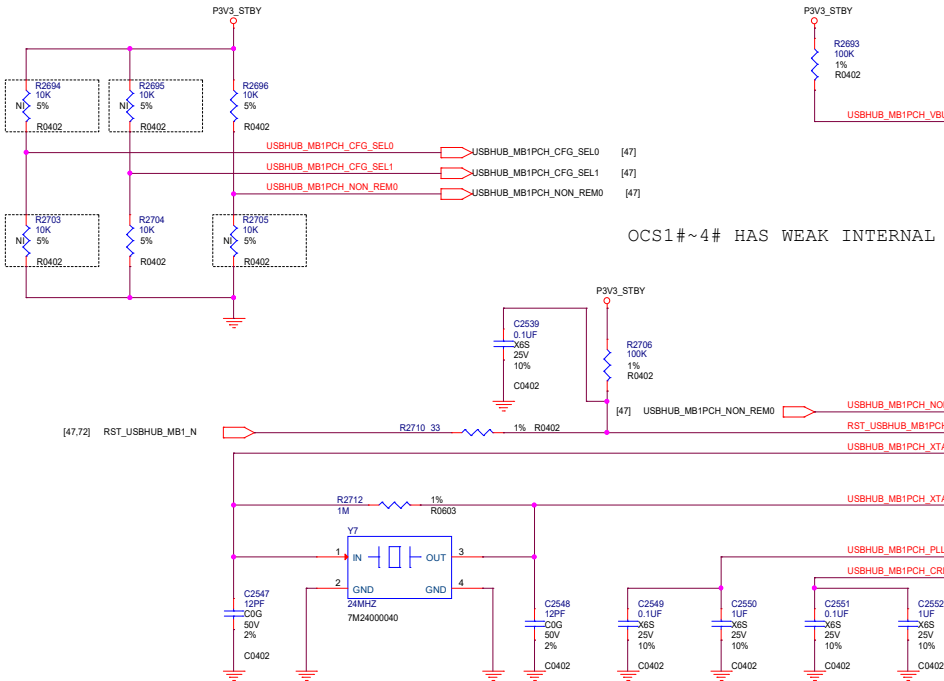
USB 2.0 HUB FOR MB0 BMC



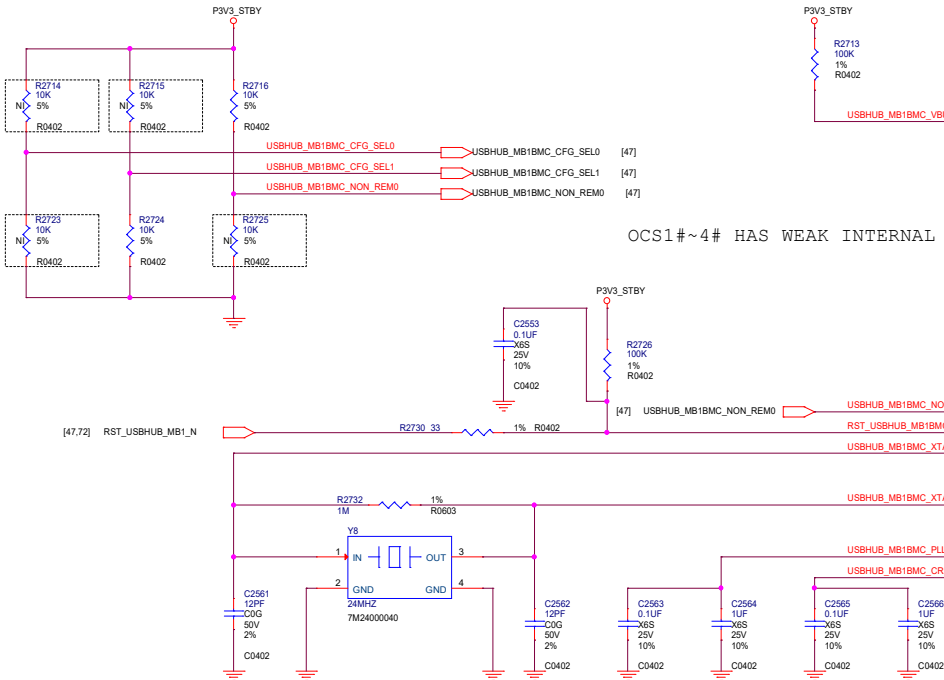
USB HUB MB0

OCS1#~4# HAS WEAK INTERNAL PU

USB 2.0 HUB FOR MB1 PCH



USB 2.0 HUB FOR MB1 BMC

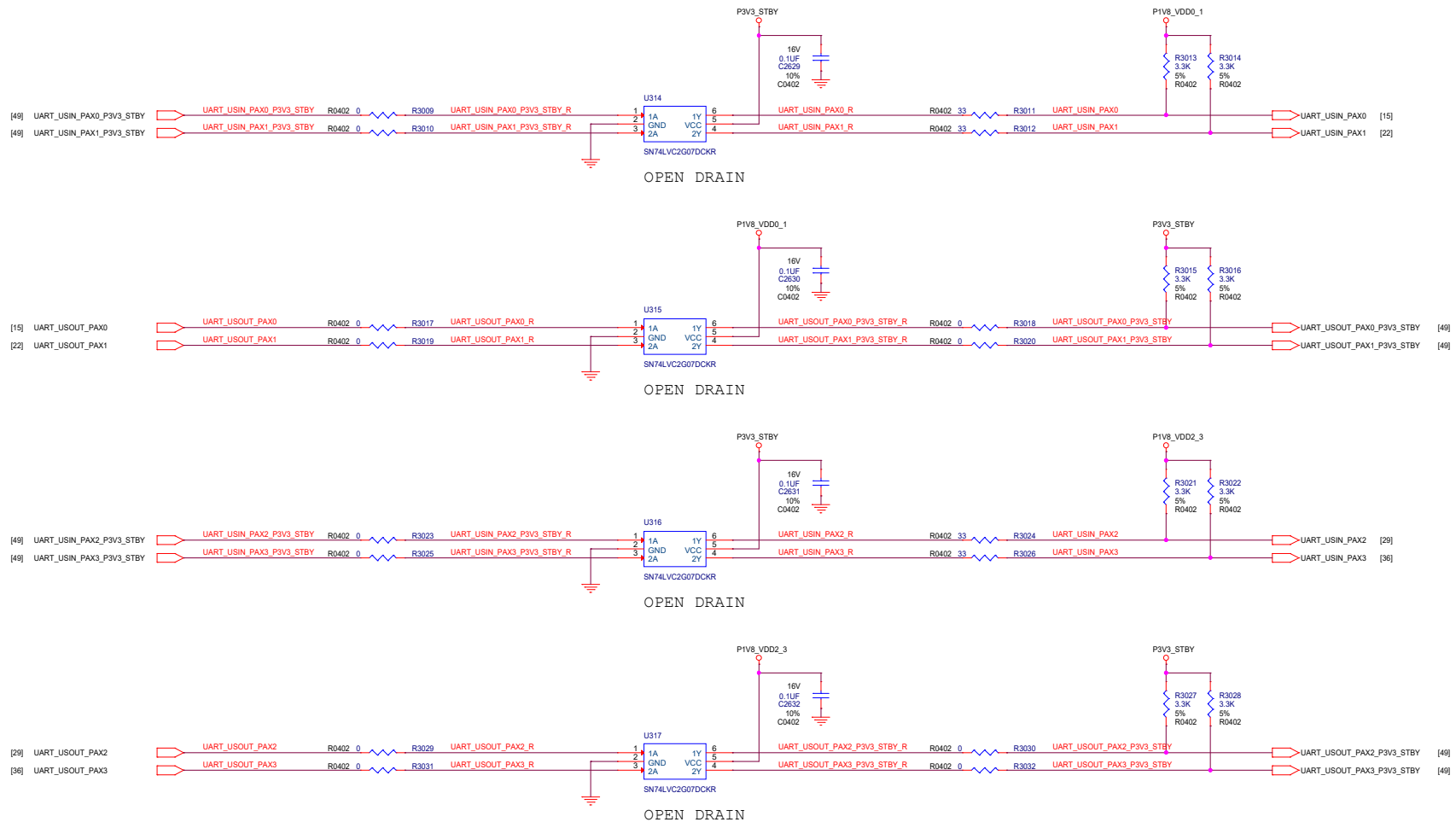


HUB ADDRESS : 0X58

HUB ADDRESS : 0X58

USB HUB MB1

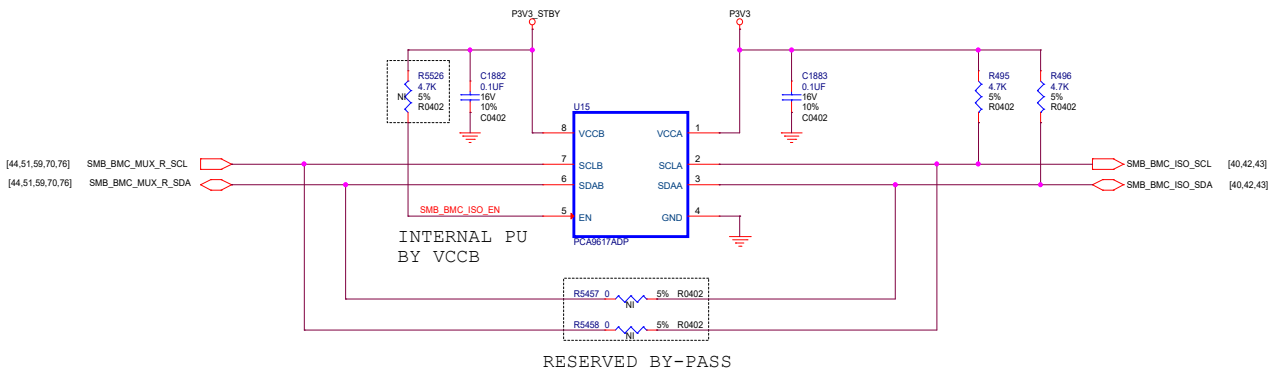
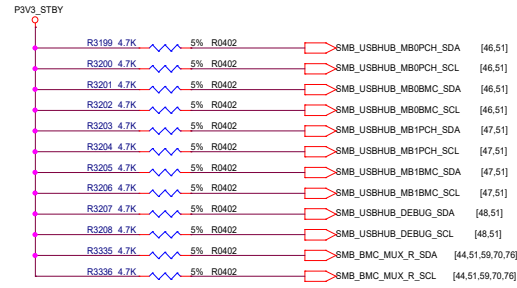
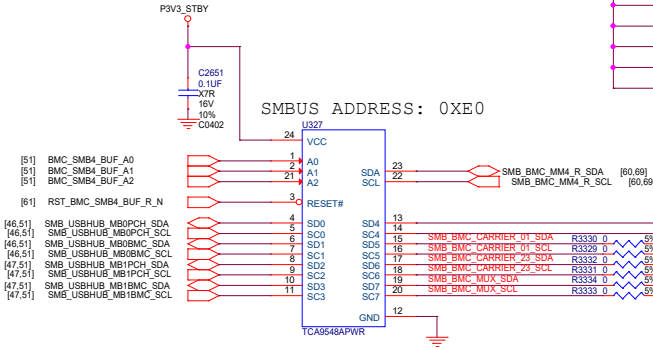
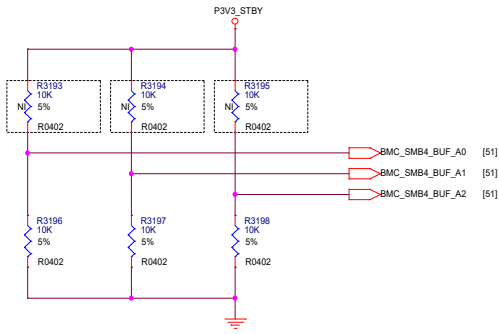

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Design Note:
1. Level shifter
2. Prevent power leakage
```

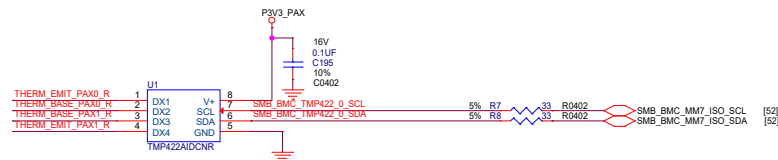
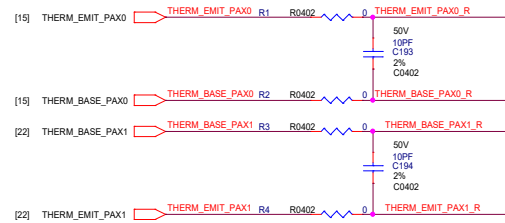


PAX UART BUFFER

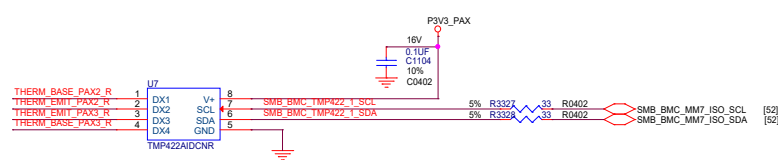
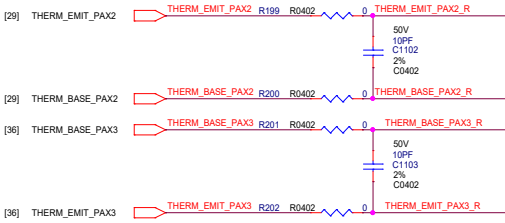
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		Reviewer	Size	Page Title	Sheet of
		<Reviewer>	Wednesday, September 20, 2023	PAX UART BUFFER	50 of 173

BMC SMB MUX

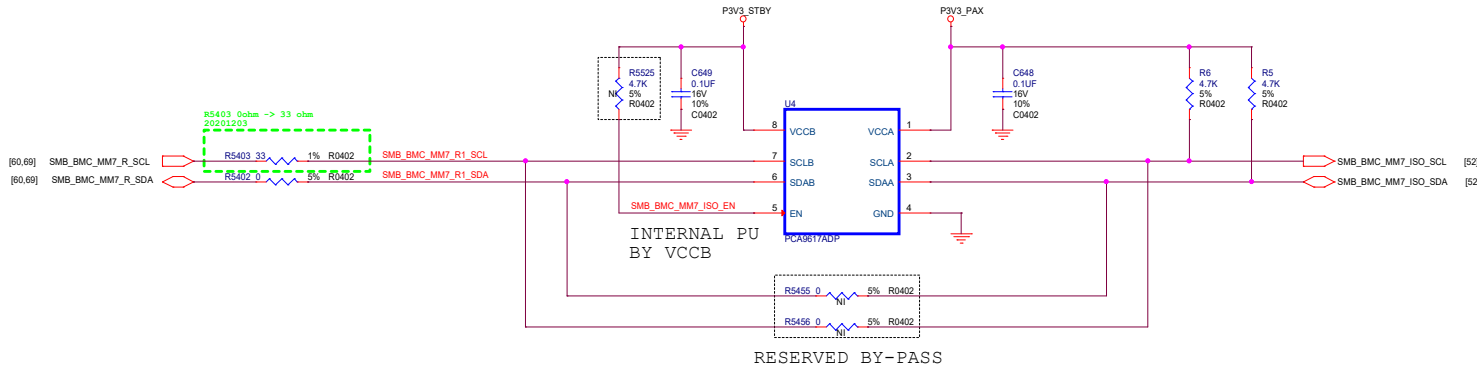




PAX DIE THERMAL SENSOR (ADDRESS: 0X9A)



PAX DIE THERMAL SENSOR (ADDRESS: 0X9C)

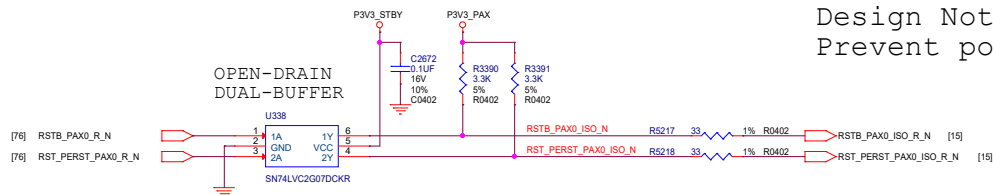


RESERVED BY-PASS

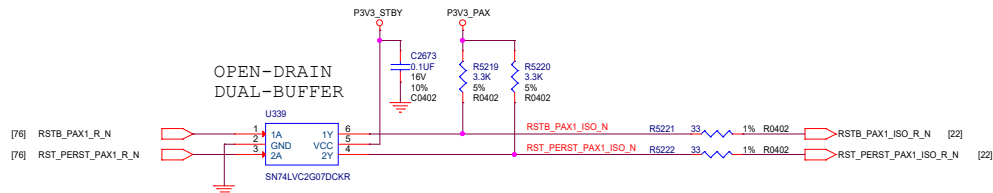
PAX THERMAL SENSOR

Design Note: Prevent power leakage

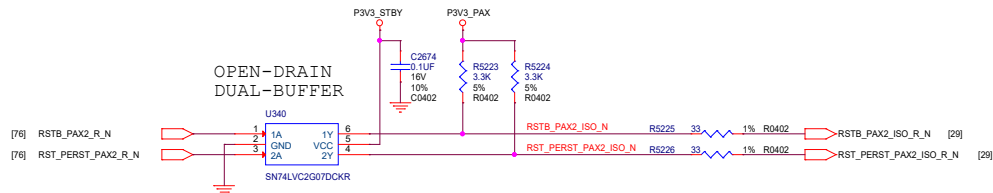
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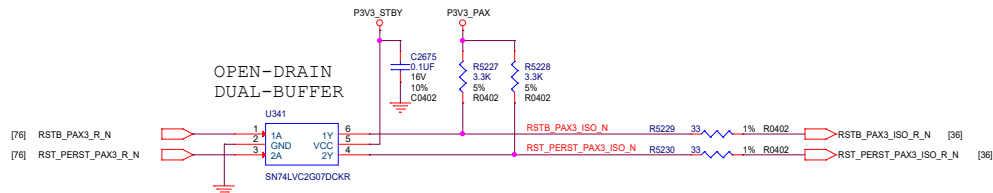
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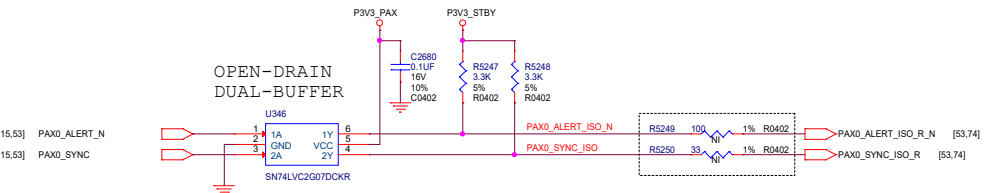
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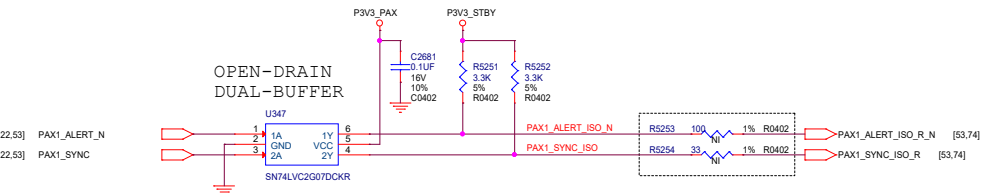
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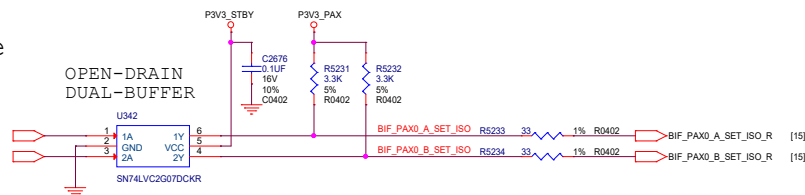
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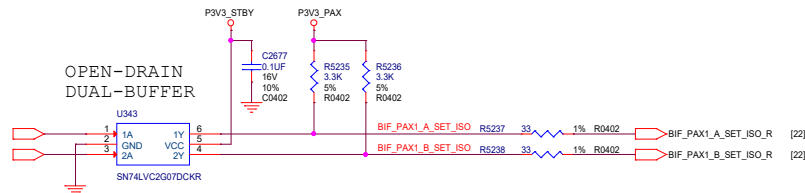
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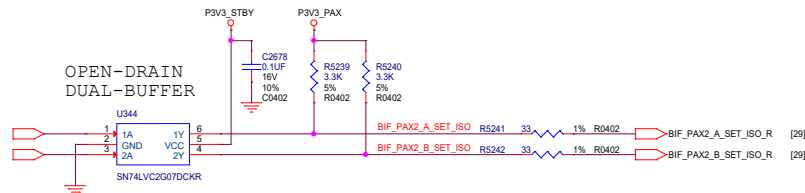
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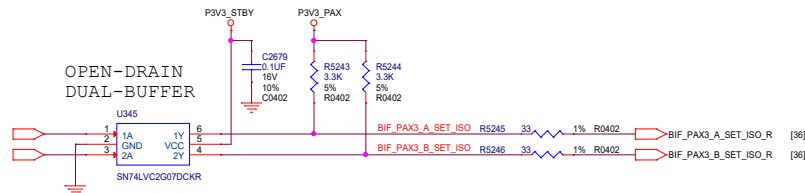
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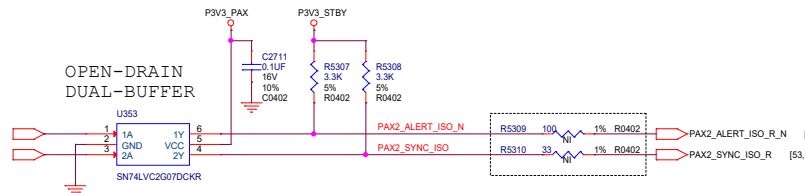
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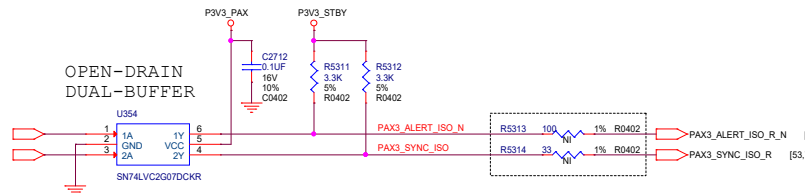
OPEN-DRAIN DUAL-BUFFER



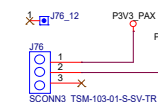
OPEN-DRAIN DUAL-BUFFER



OPEN-DRAIN DUAL-BUFFER

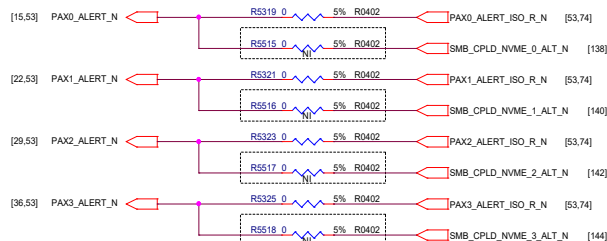
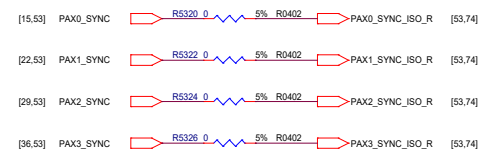


CAD NOTE
P3V3_PAX_LED at least 20 mil.

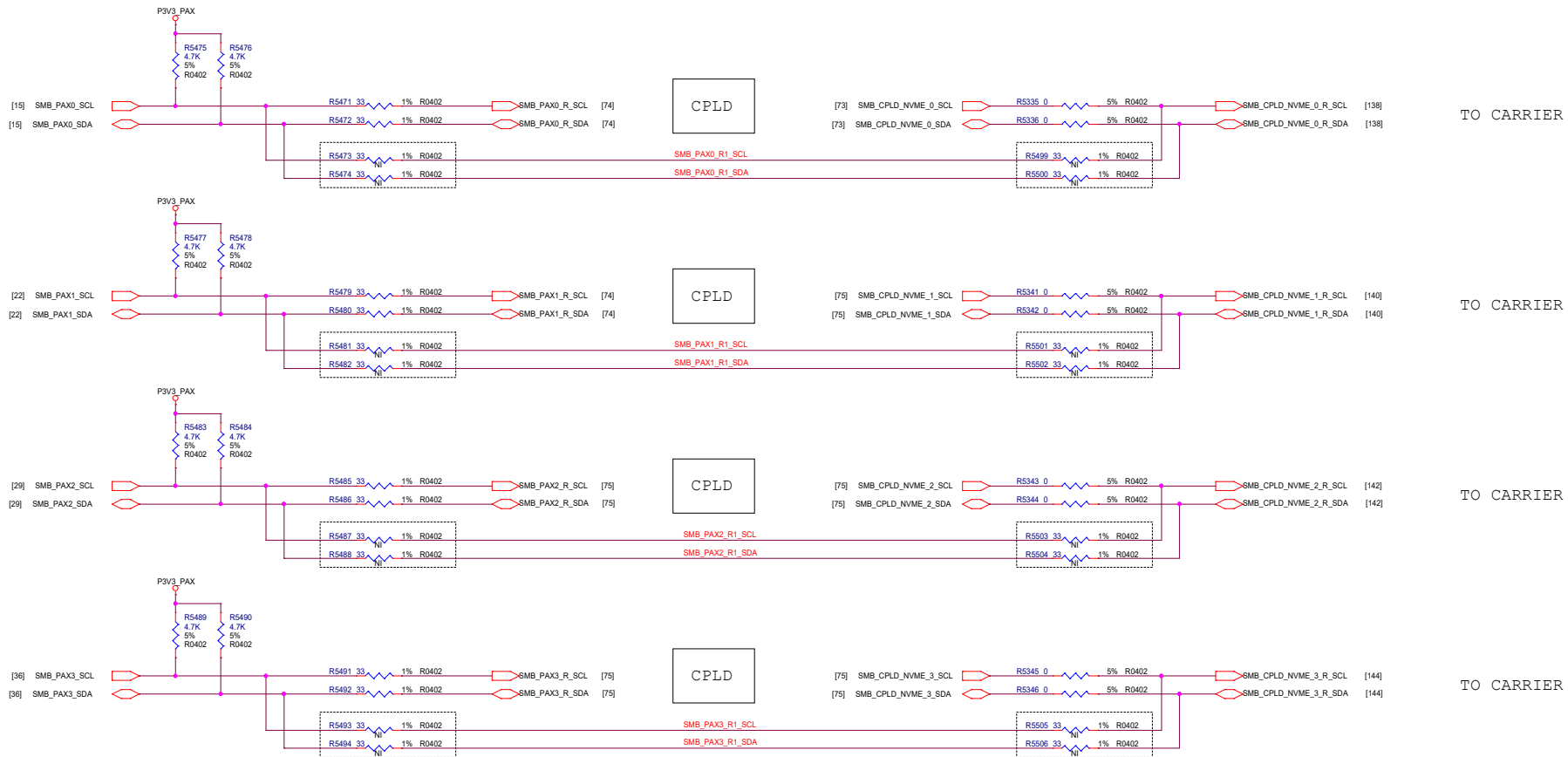


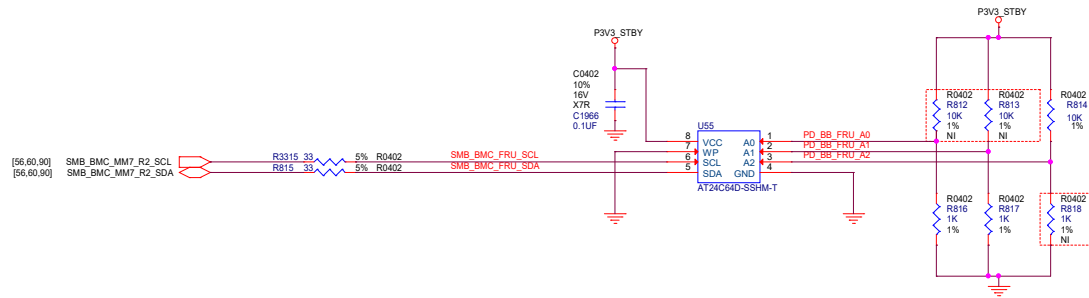
PAX LED Heart Beat Debug Purpose
Jumper(1-2) : Enable LED
Jumper(2-3) : Disable LED

Reserve for By-pass

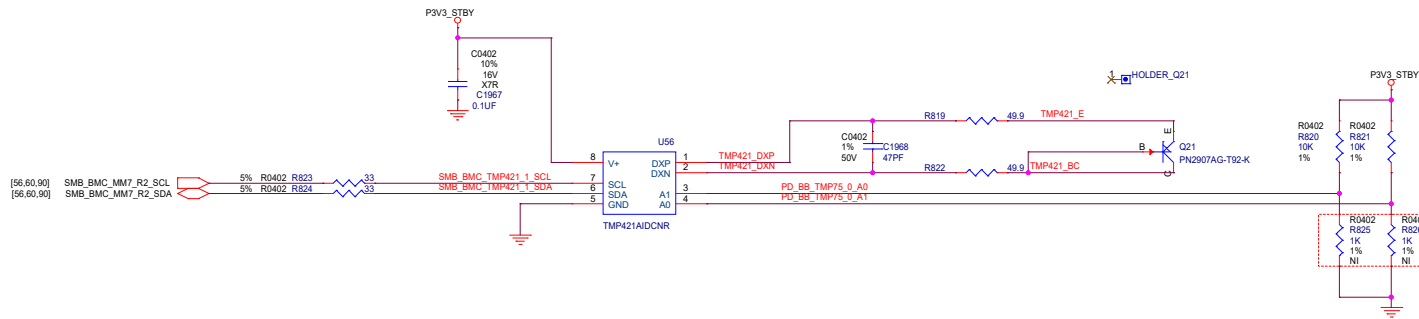


PAX IOSLATION(2/2)

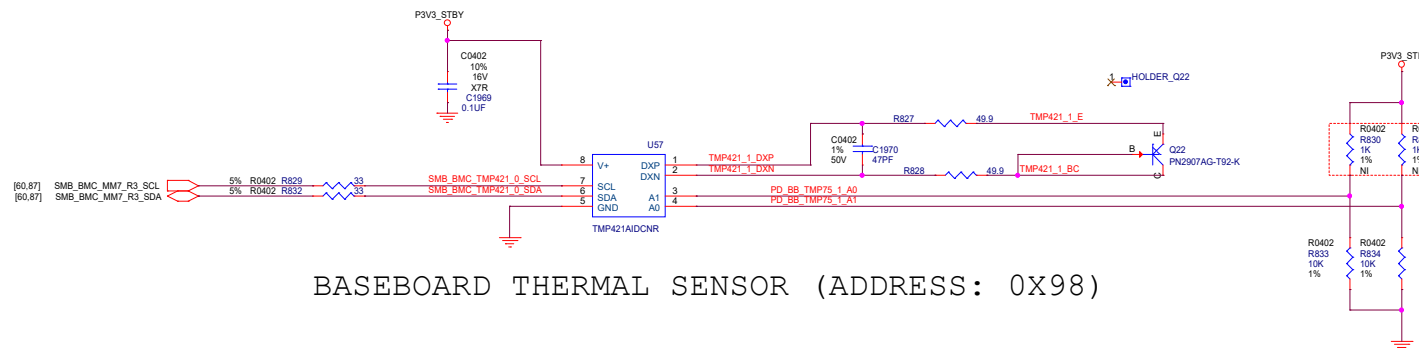




BASEBOARD FRU (SMB9 ADDRESS: 0XA8)



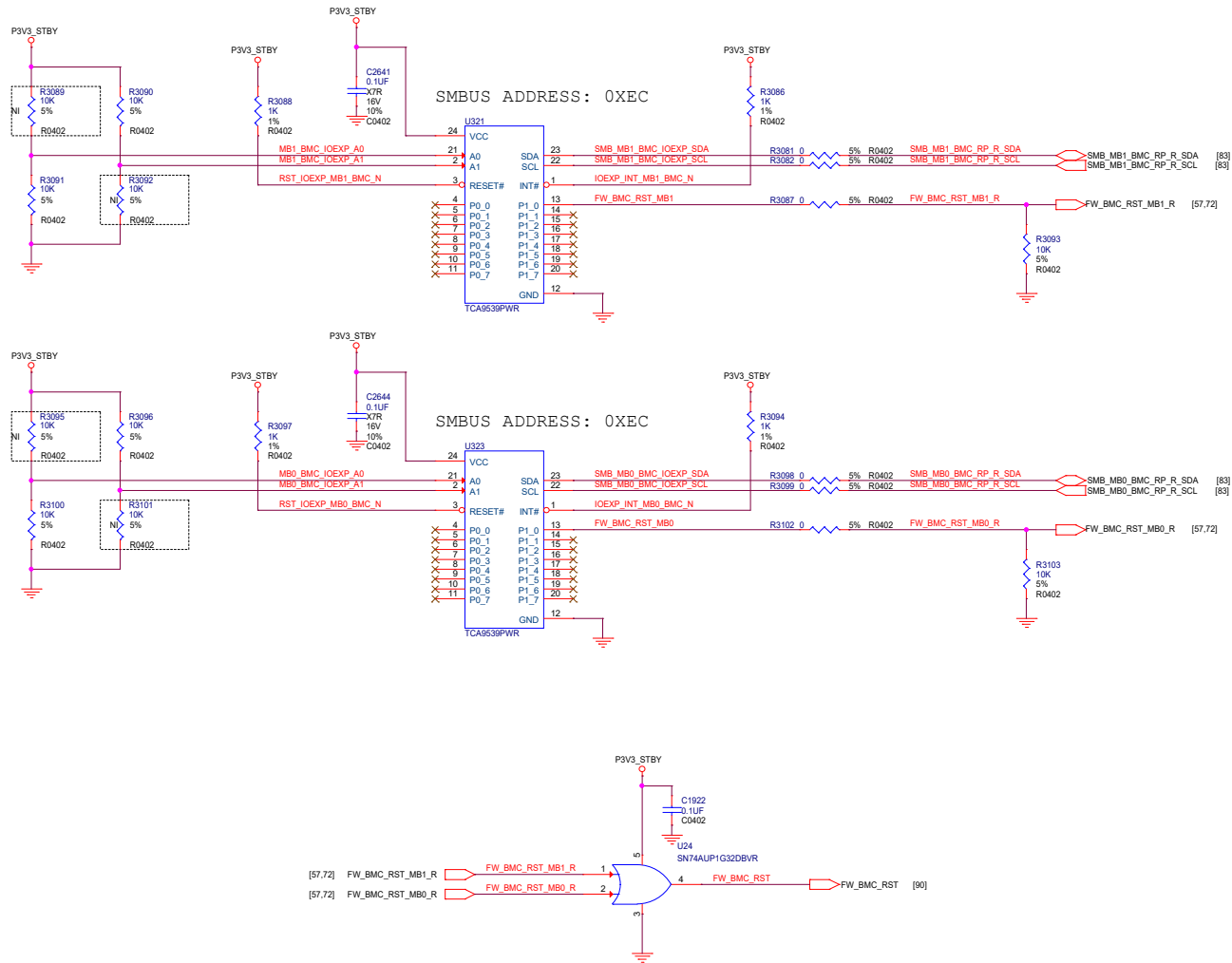
BASEBOARD THERMAL SENSOR (ADDRESS: 0X9E)



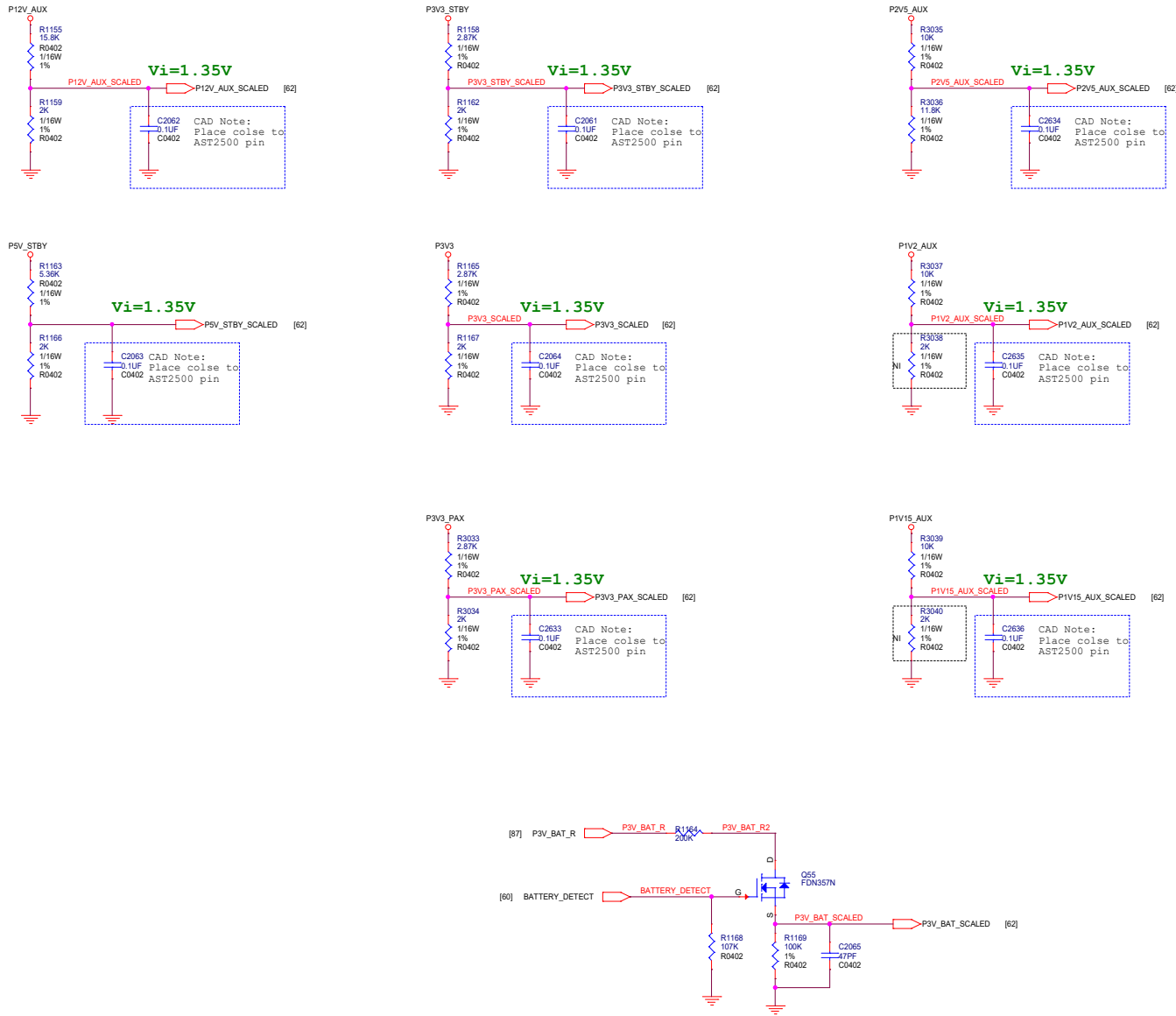
BASEBOARD THERMAL SENSOR (ADDRESS: 0X98)

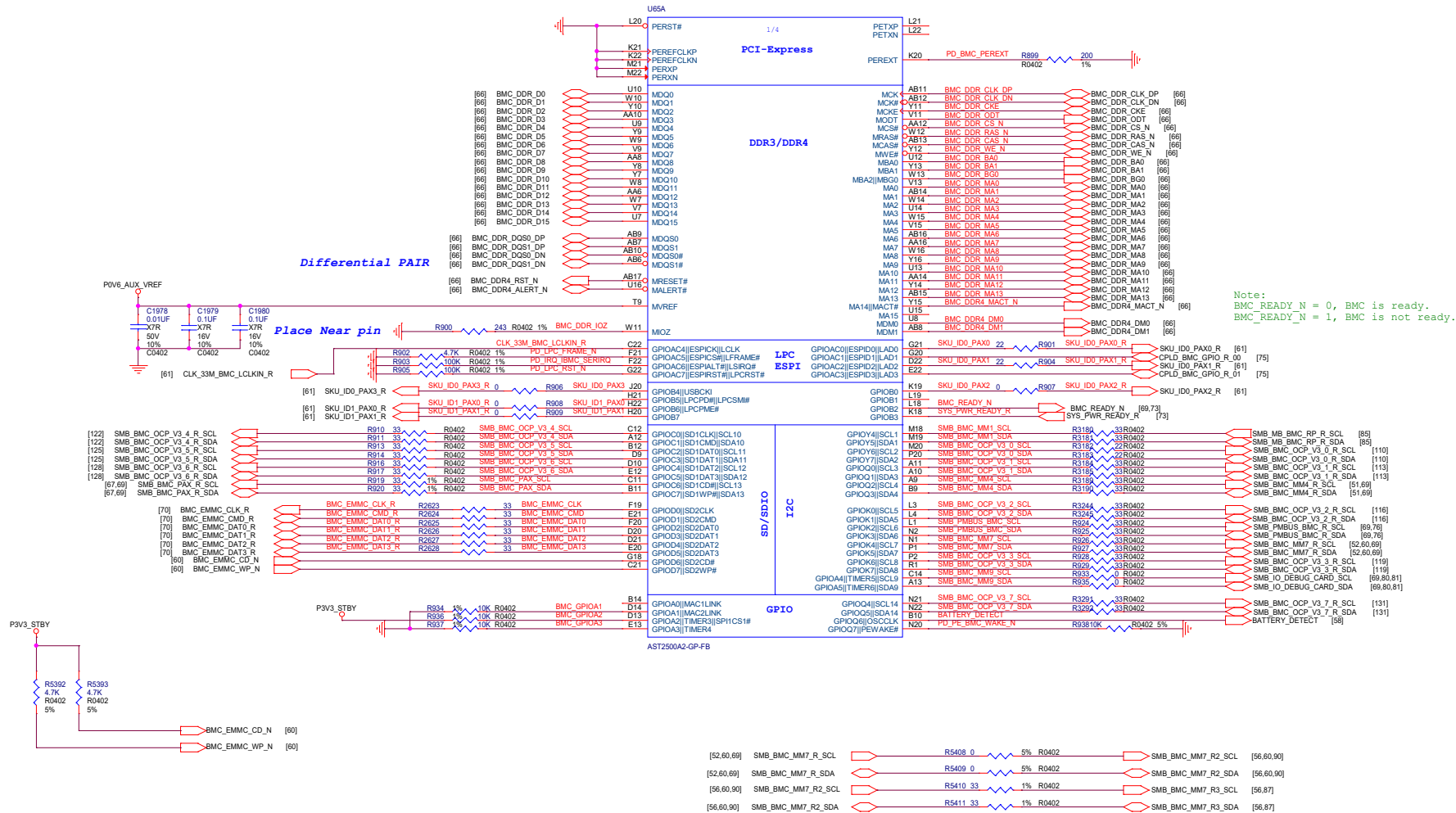
BASEBOARD_FRU_TEMP_SENSOR

BMC IO EXP

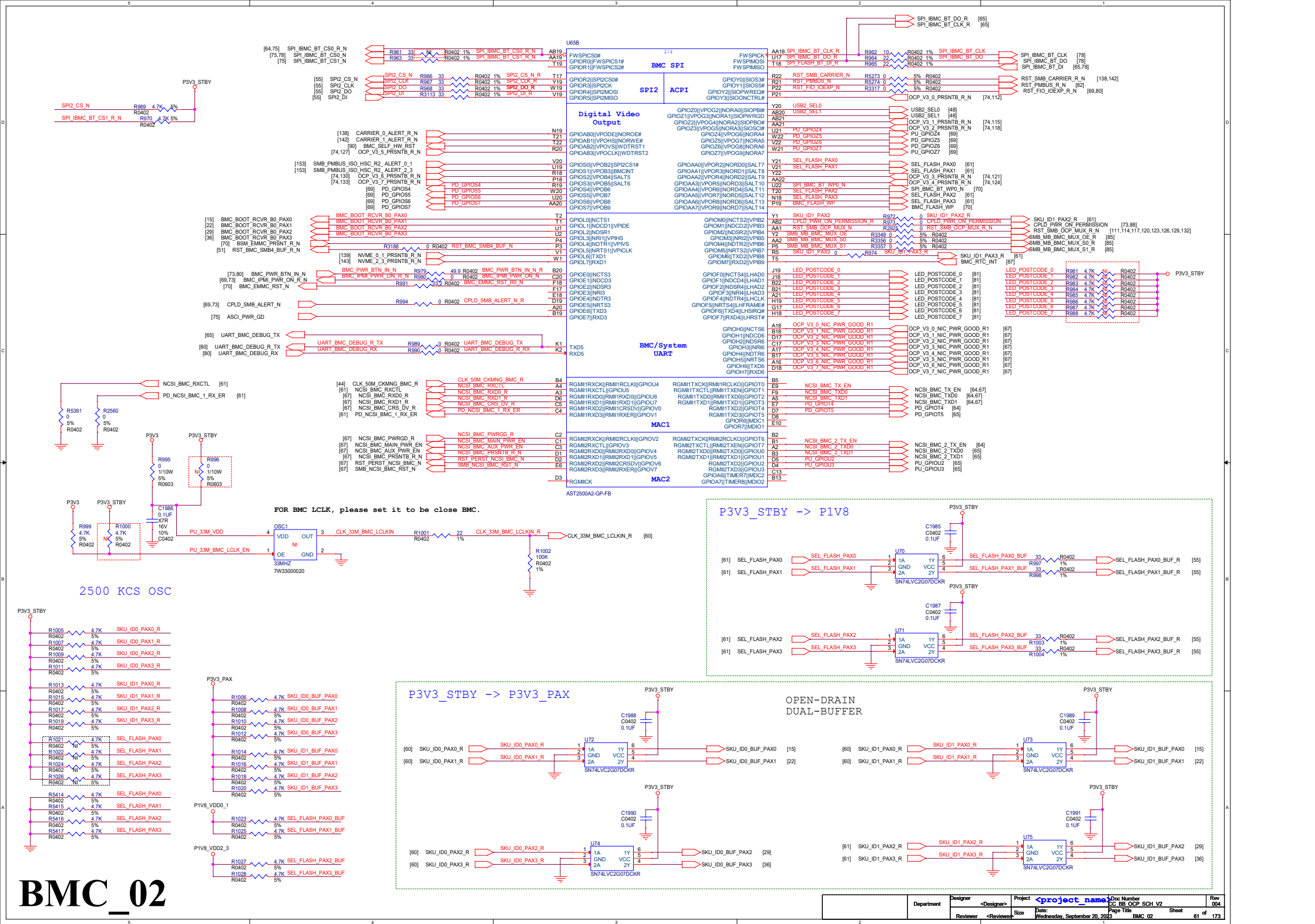


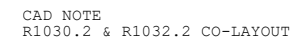
ROUTE ALL ADC NETS AT 6 MILLS WIDE

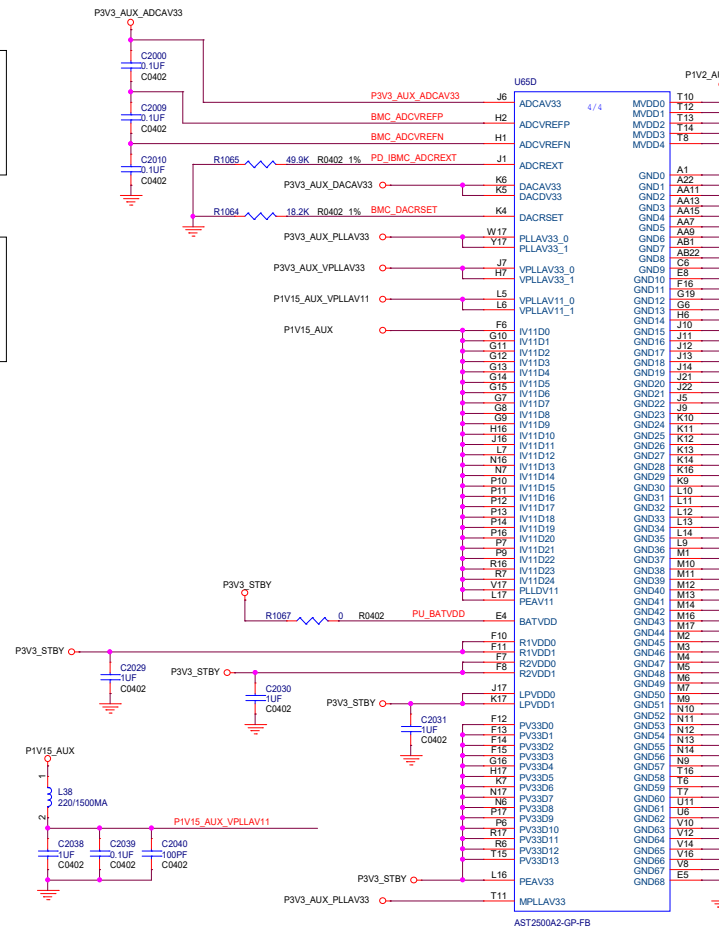
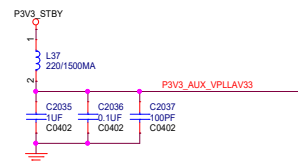
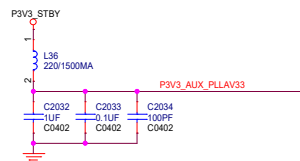
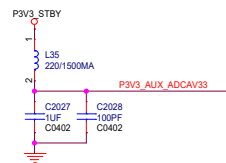
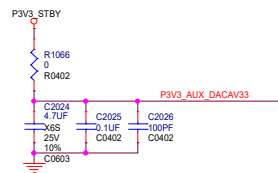
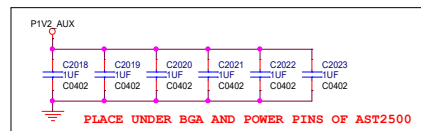
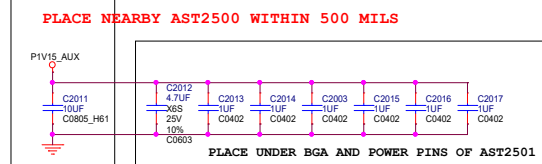
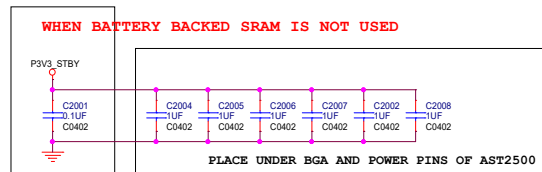


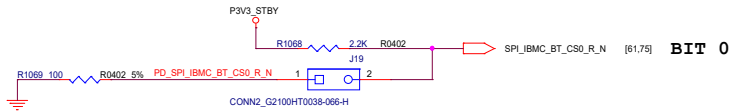


Note:
BMC_READY_N = 0, BMC is ready.
BMC_READY_N = 1, BMC is not ready.



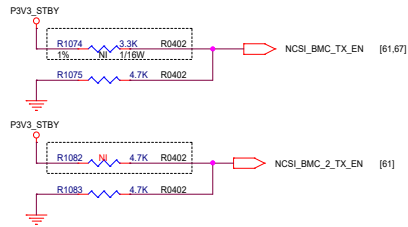




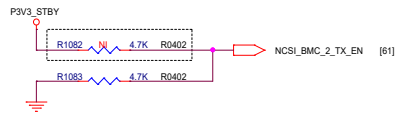


GPIO strap pins definition.

Pin	Definition	Value = 0	Value = 1	Valid for PN
GPIO4	VGA memory size selection	16 MB	64 MB	2500/2530
GPIO5	Reserved	Default	Disallowed	2500/2530
GPIO6	Enable VGA BIOS ROM	No	Yes	2500/2530
GPIO7	VGA Class Code selection	Non-VGA	VGA	2500/2530
GPIOZ4	Enable BMC 2nd boot watchdog timer	No	Yes	2500/2520/2530
GPIOZ5	Select USBCKI input frequency	24MHz	48MHz	2500/2520/2530
GPIOZ6	Disable LPC to decode SuperIO address	No	Yes	2500/2520/2530
GPIOZ7	Enable fast reset mode	No	Yes	2500/2520/2530

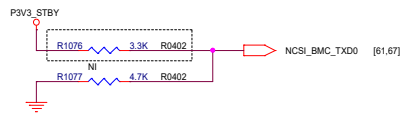


BIT 6



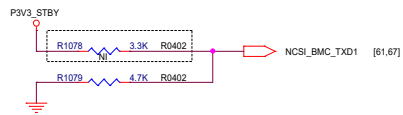
BIT 7

short routing stub



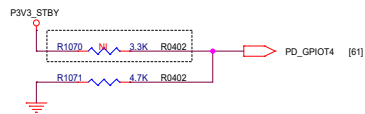
BIT 12

short routing stub



BIT 13

short routing stub



BIT 16

BIT 0 (DEDICATED STRAP PIN)
BALL NAME: FWSPIC0#
*0=ENABLE BMC
1=DISABLE BMC

BIT 1 (NOT IN HW STRAP)
RESERVED

BIT 2 (OPTIONAL STRAP PIN)
VGA MEMORY SIZE SELECTION

BIT 3 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO4

BIT 4 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO5

BIT 5 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO6
0=NO VGA BIOS ROM,VGA BIOS IS MERGED IN THE SYSTEM BIOS
1=ENABLE DEDICATED VGA BIOS ROM

BIT 6 (DEDICATEDL STRAP PIN)
BALL NAME: RGMIIITXCTL
*0=RMII/NCSI
1=RGMI

BIT 7 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII2TXCTL
0=RMII/NCSI
*1=RGMI

BIT 8 (NOT IN HW STRAP)
CPU/AXI CLOCK FREQUENCY RATIO SELECTION
0=SELECT CPU/AXI= 1:1
1=SELECT CPU/AXI= 2:1

BIT 11:9 (NOT IN HW STRAP)
AXI/AHB CLOCK FREQUENCY RATIO SELECTION
000=UNDEFINED
001=SELECT AXI:AHB= 2:1
010=SELECT AXI:AHB= 3:1
011=SELECT AXI:AHB= 4:1
100=SELECT AXI:AHB= 5:1
101=SELECT AXI:AHB= 6:1
110=SELECT AXI:AHB= 7:1
111=SELECT AXI:AHB= 8:1

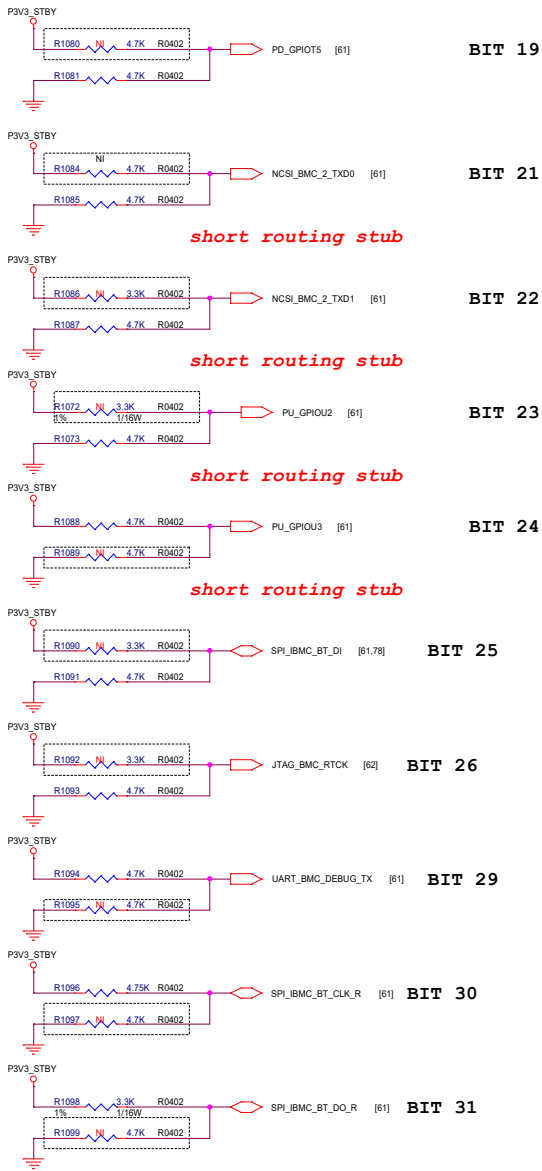
BIT 12 (DEDICATEDL STRAP PIN)
BALL NAME: RGMIIITXD0
BIT 13 (DEDICATEDL STRAP PIN)
BALL NAME: GPLOT3

*00=DISABLE SPI INTERFACE
01=ENABLE SPI MASTER
10=ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE
11=ENABLE SPI PASS-THROUGH

BIT 14 (NOT IN HW STRAP)
SELECT DEDICATED LPC RESET INPUT
0=LPC RESET IS SHARED WITH PCIE RESET PIN
1=LPC RESET IS LOCATED AT PIN NUMBER G22,SHARED WITH GPIOAC7

BIT 15 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO7
0=SELECT THE CLASS CODE FOR VIDEO DEVICE
1=SELECT THE CLASS CODE FOR VGA DEVICE

BIT 16 (DEDICATED STRAP PIN)
BALL NAME: GPLOT4
*0=DECODE 0X2E
1=DECODE 0X4E



BIT 17 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO24
0=DISABLE
1=ENABLE BMC 2ND BOOT WATCHDOGTIMER START COUNTING AT POWER UP.

BIT 18 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO25
0=24MHz
1=48MHz

BIT 19 (DEDICATED STRAP PIN)
BALL NAME: GPIOTS
*0=DISABLE ACPI
1=ENABLE ACPI

BIT 20 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO26
0=ENABLE ADDRESS DECODING
1=DISABLE ADDRESS DECODING

BIT 21 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD0
*0=DISABLE PASS THROUGH CAN BE ENABLED BY SCU8C[11:8]
1=ENABLE PASS-THROUGH AT POWER ON.
GPIO0 -> GPIO1
GPIO2 -> GPIO3
GPIO4 -> GPIO5
GPIO6 -> GPIO7

BIT 22 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD1
*0=DISABLE PASS THROUGH CAN BE ENABLED BY SCU8C[15:12]
1=ENABLE PASS-THROUGH AT POWER ON.
GPIO0 -> GPIO1
GPIO2 -> GPIO3
GPIO4 -> GPIO5
GPIO6 -> GPIO7

BIT 23 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD2
*0=CLKIN IS 24 MHZ AND USBCKI NOT USED
1=CLKIN IS 25 MHZ AND USBCKI= 24/48 MHZ (DETERMINED BY BIT[18])

BIT 24 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD3
0=DDR3 SDRAM
*1=DDR4 SDRAM

BIT 25 (DEDICATED STRAP PIN)
BALL NAME: FWSPIMISO
0=LPC MODE (ONLY FOR PSPO STAGE)
1=ESPI MODE (NORMAL STAGE)

BIT 26 (DEDICATED STRAP PIN)
BALL NAME: RTCK
0=ESPI RESPOND W/O FLASH ATTACHED
1=ESPI RESPOND W/ FLASH ATTACHED

BIT 27 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIO27
0=LONG RESET MODE, NORMAL OPERATION
1=FAST RESET MODE, FOR ICE DEBUGGER CONNECTION

BIT 28 (NOT IN HW STRAP)
RESERVED

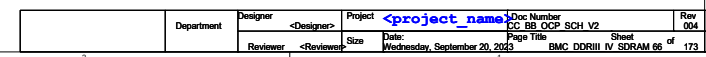
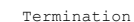
BIT 29 (DEDICATED STRAP PIN)
BALL NAME: TXD5
0=SELECT UART1 AS BMC CONSOLE PORT
1=SELECT UART5 AS BMC CONSOLE PORT

BIT 30 (DEDICATED STRAP PIN)
BALL NAME: FWSPICK
0=DISABLE
1=ENABLE

BIT 31 (DEDICATED STRAP PIN)
BALL NAME: FWSPIMOSI
0=DISABLE
*1=ENABLE

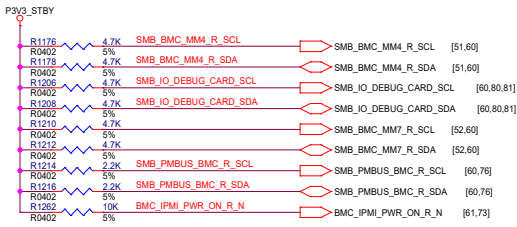
BMC_HW_STRAPPING_2

Department	Designer	Project	Doc Number	Rev
	Reviewer	Size	Date	004
			Wednesday, September 20, 2023	
			Page Title	Sheet
			BMC_HW_STRAPPING_265	173

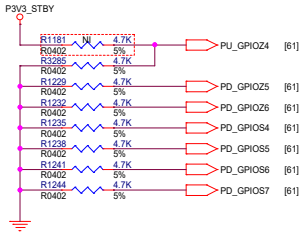
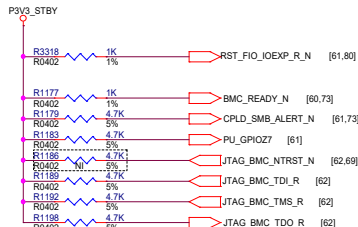


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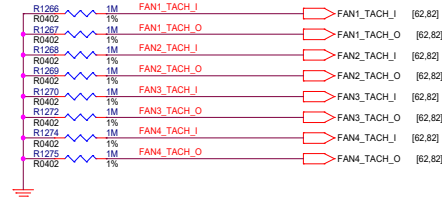
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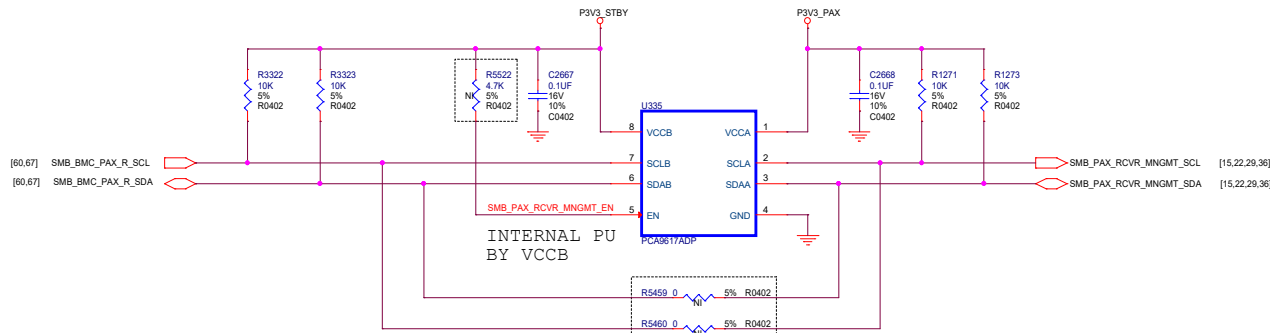
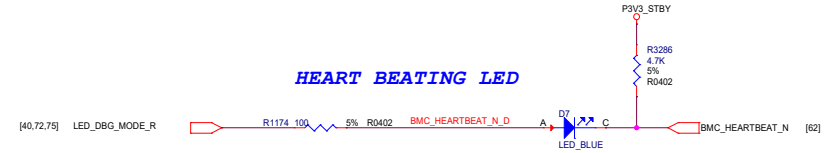
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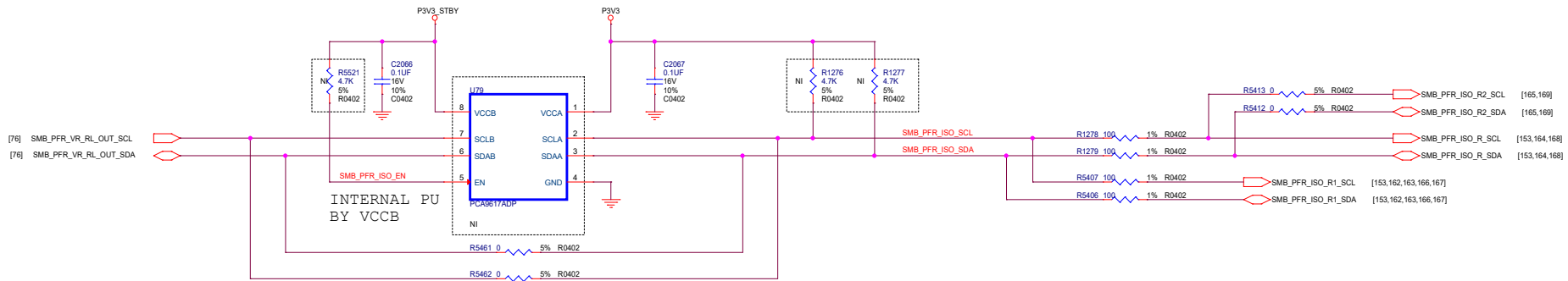
PD OF FAN TACH



HEART BEATING LED



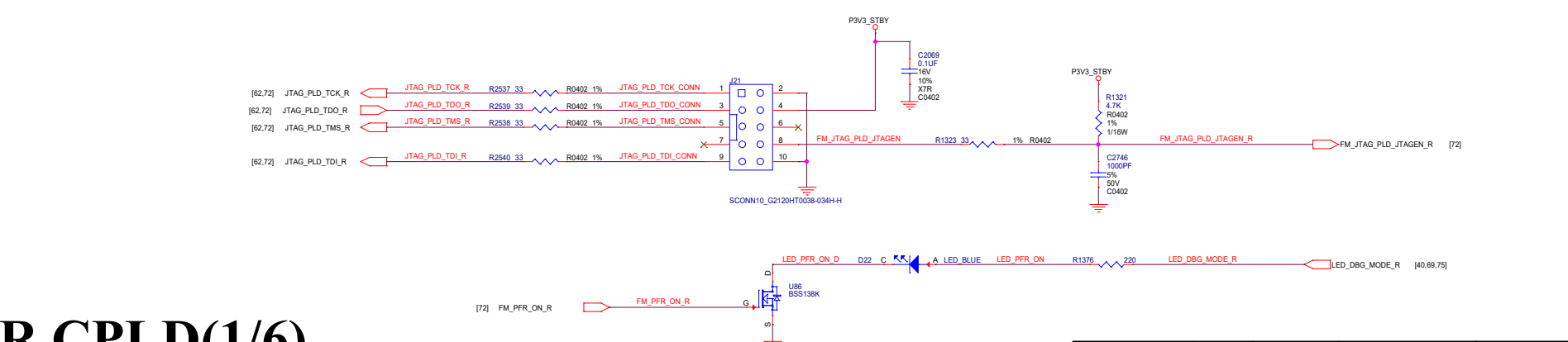
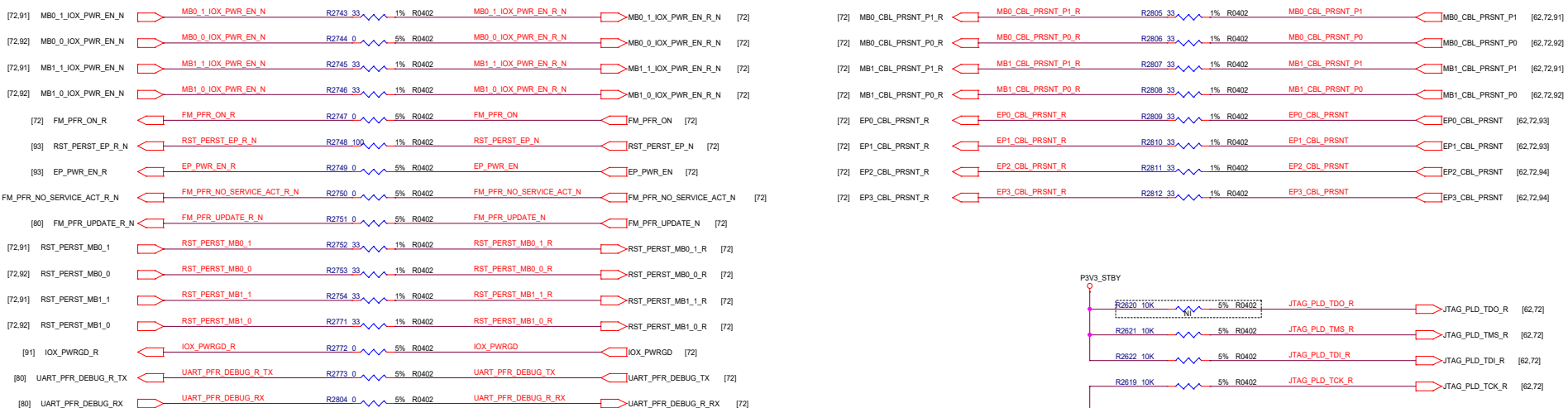
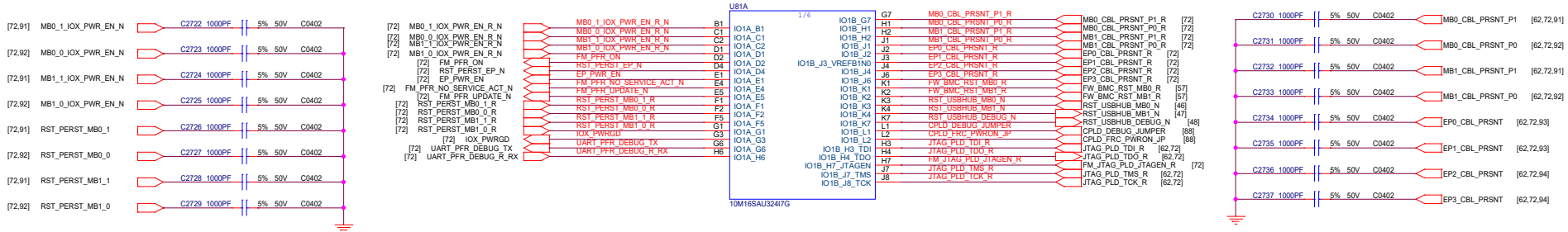
RESERVED BY-PASS



RESERVED BY-PASS

BMC&CPLD PULL UP

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PFR CPLD(1/6)

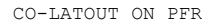
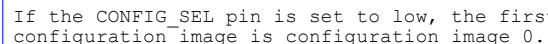


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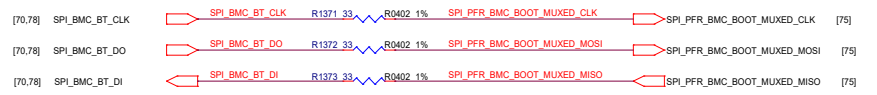
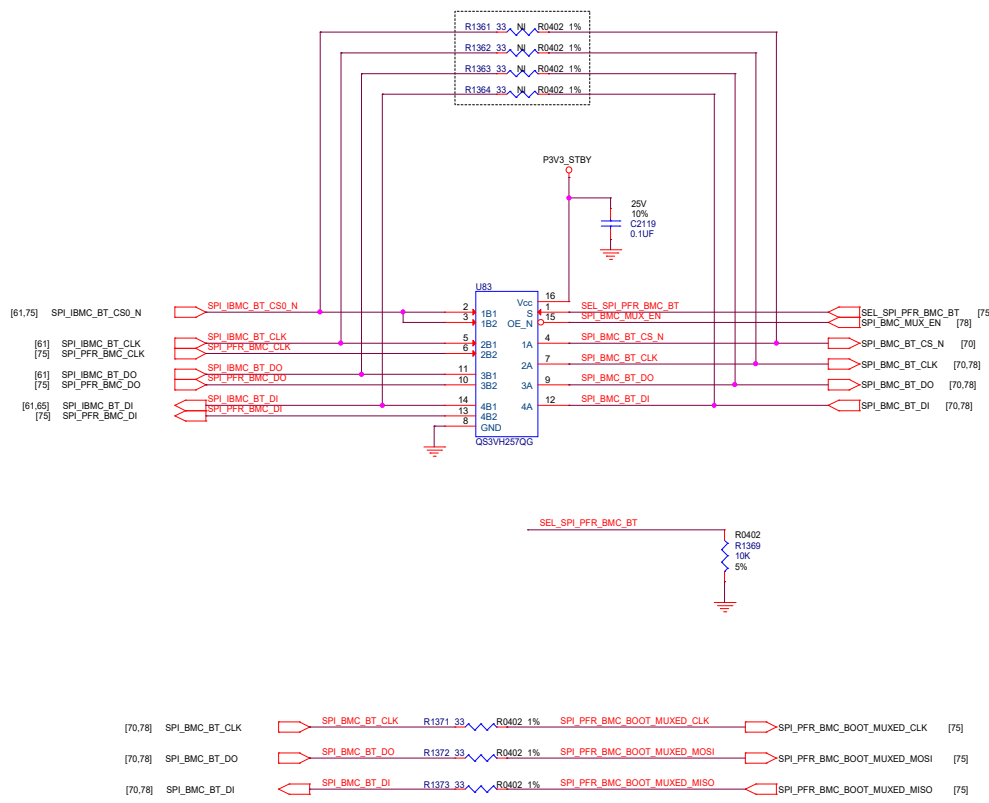
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PFR CPLD(3/6)

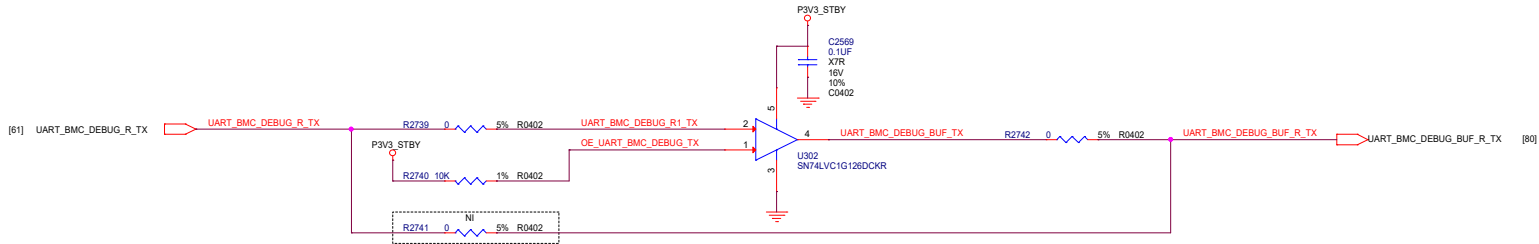
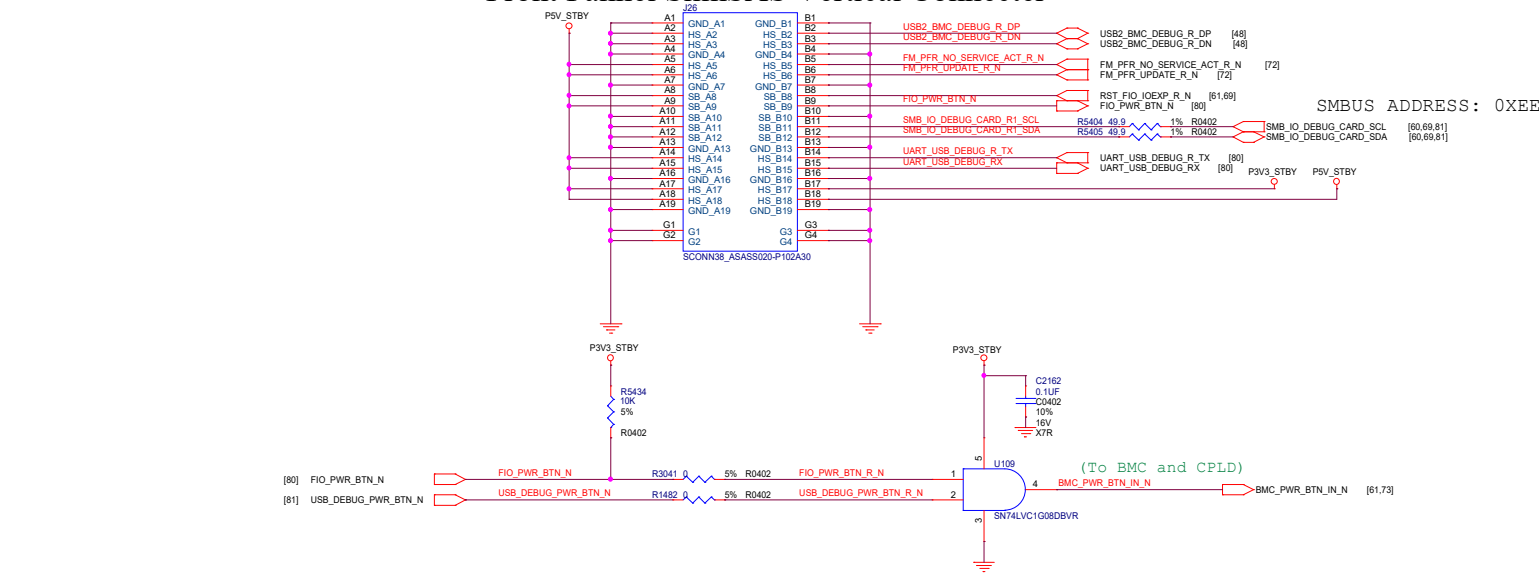


PFR SPI

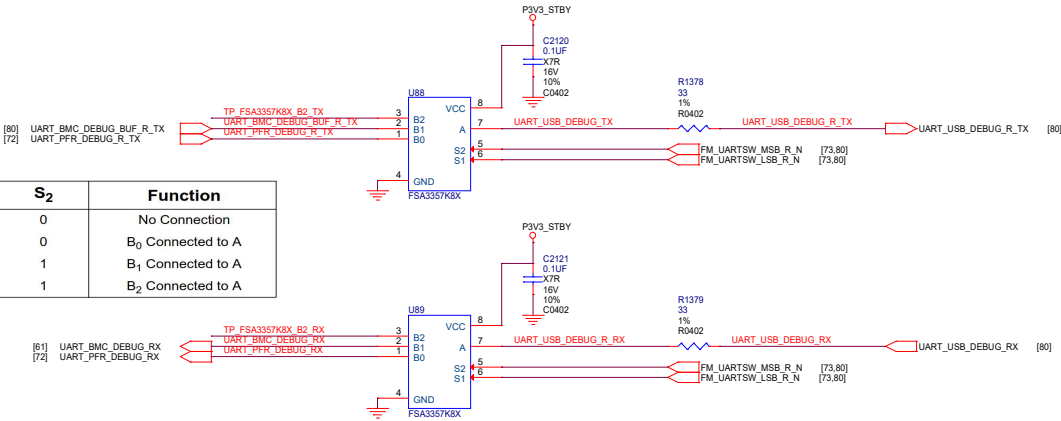


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Front Pannel SlimSAS Vertical Connector

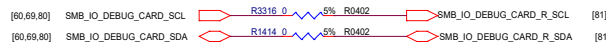


Follow Sonora Pass to solve glitch issue when system default is BMC mode.
When choose PFR mode as default, pop R2741 and depop U302 and R1094.



S ₁	S ₂	Function
0	0	No Connection
1	0	B ₀ Connected to A
0	1	B ₁ Connected to A
1	1	B ₂ Connected to A

FRONT PANNEL



slave address

0	1	0	0	A2	A1	A0	R/W
---	---	---	---	----	----	----	-----

fixed hardware selectable

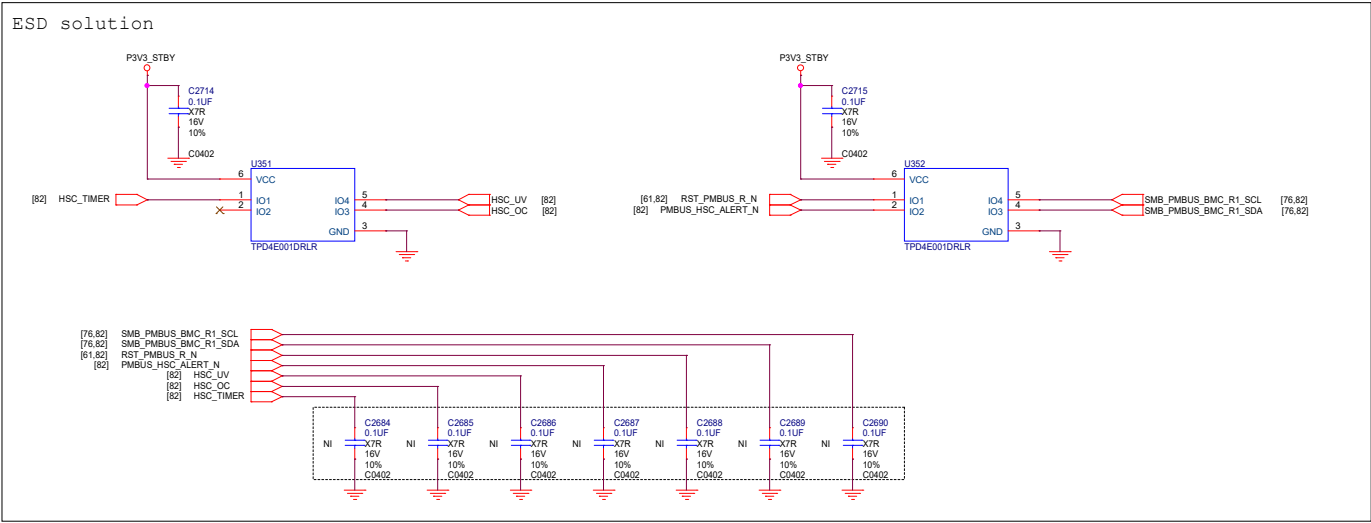
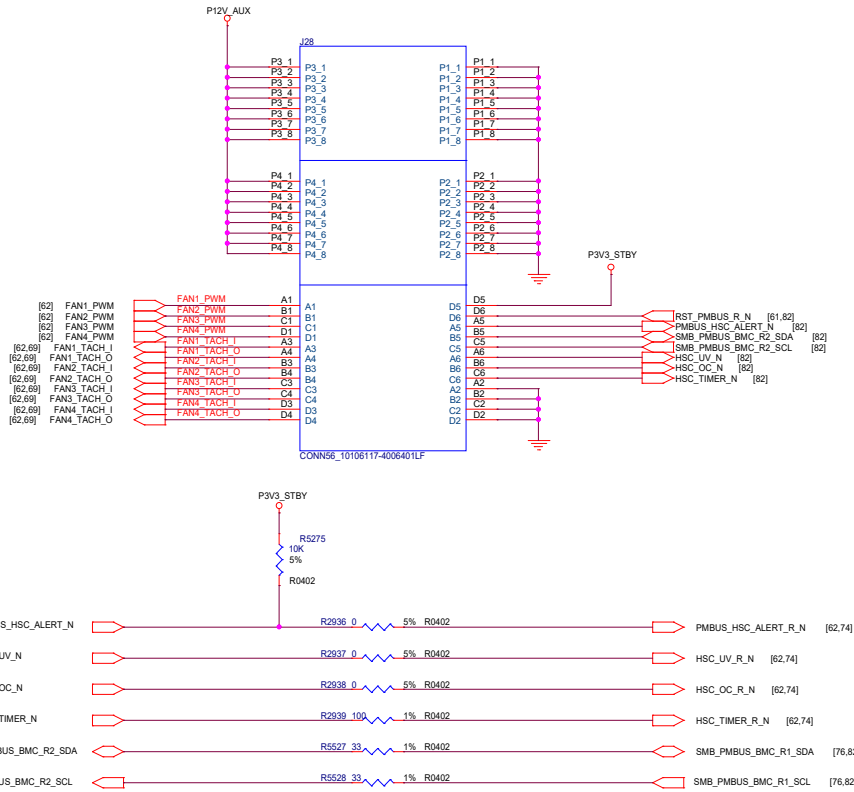
0	1	0	0	1	1	1
---	---	---	---	---	---	---

I2C address: 0x4E

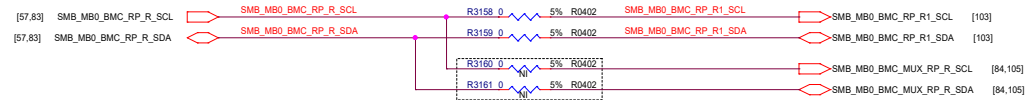
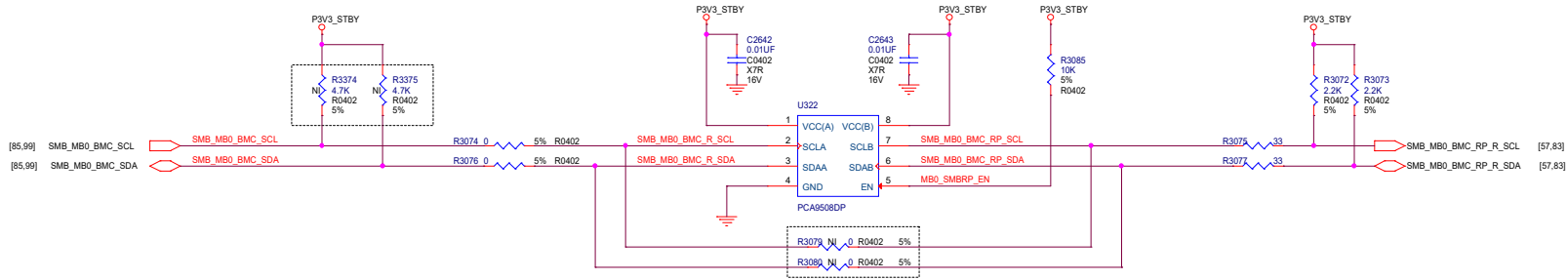
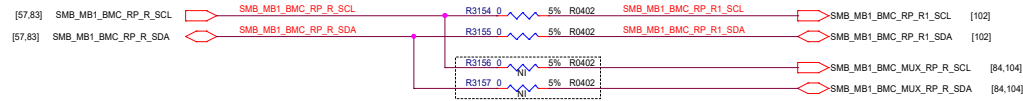
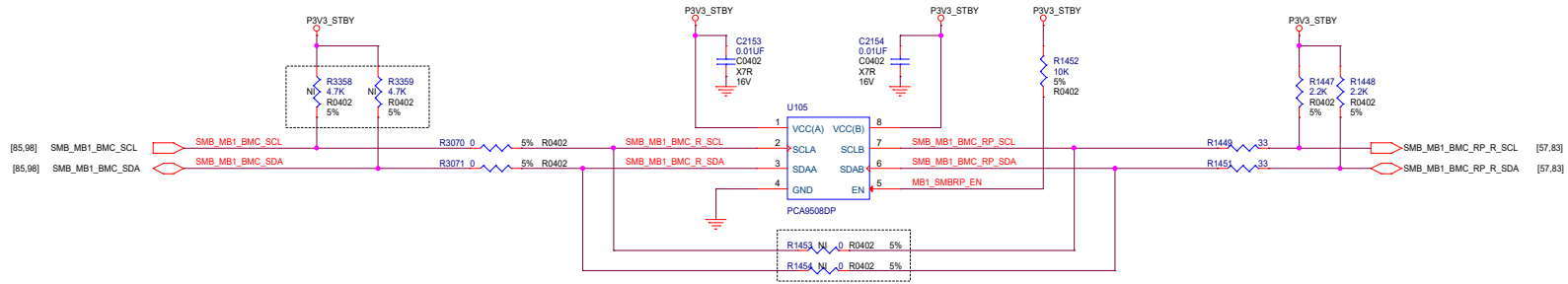
P3V3_STBY

R1418 10K	USB_DEBUG_RST_BTN_N
10K R4002	
R1420 50K	USB_DEBUG_PWR_BTN_N
10K R4002	
R1421 10K	FM_SOL_UART_CH_SEL
10K R4002	
R1422 50K	PWRGD_DSW PWROK
10K R4002	
R1423 50K	PWRGD_SYS_PWROK
10K R4002	
R1424 50K	RST_PLTRST_N
10K R4002	
R1425 50K	FM_CPU_CATERR_MSMI_LV173_N
10K R4002	
R1429 50K	FM_SLPS3_N
10K R4002	

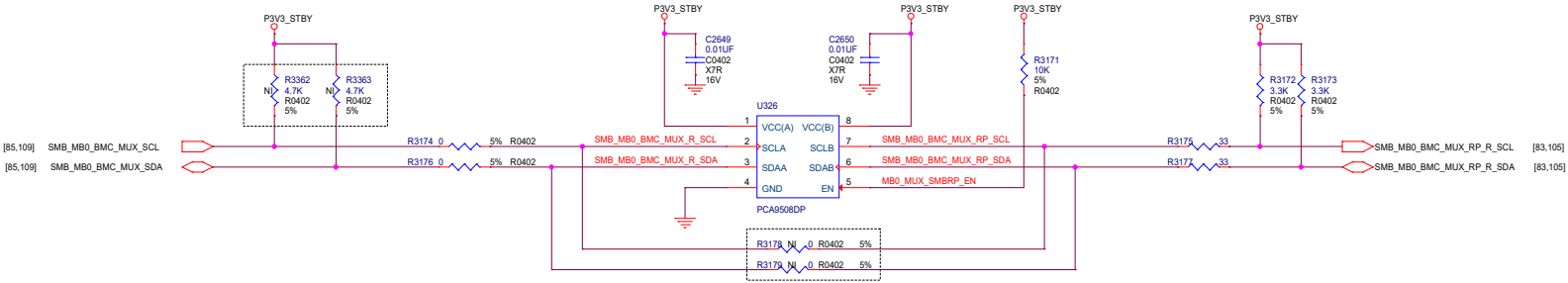
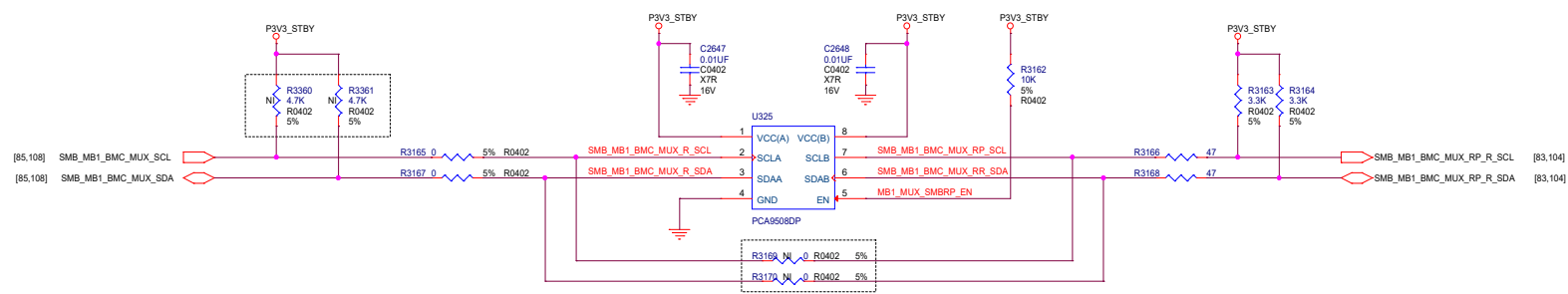
USB DEBUG



PWR CONN

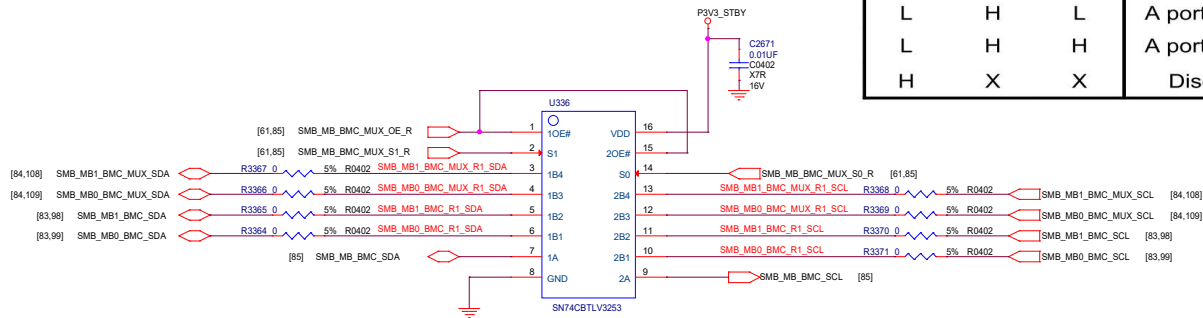
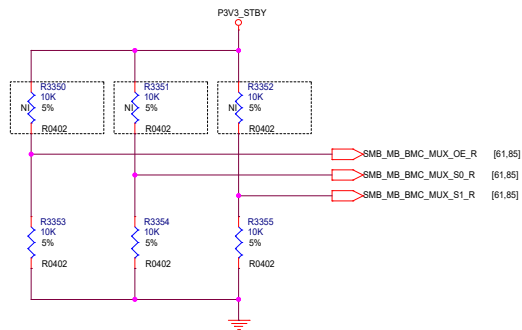
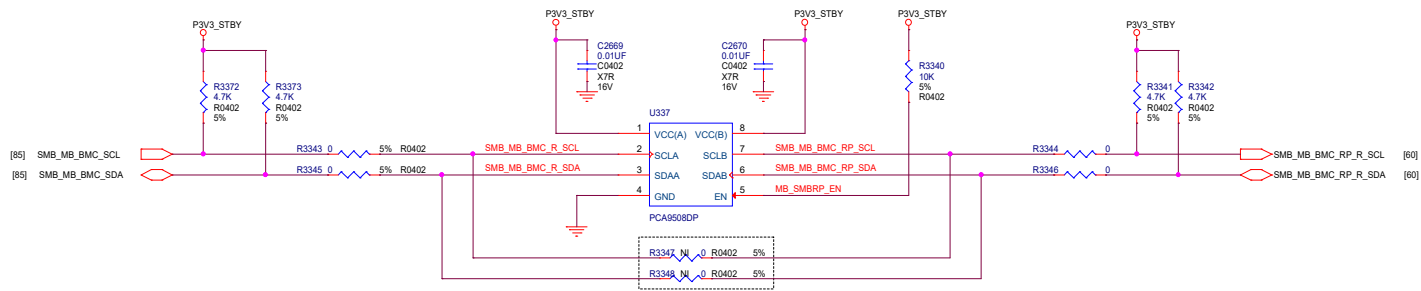


SMBUS REPEATER(1/3)



SMBUS REPEATER(2/3)

SMBUS REPEATER(3/3)

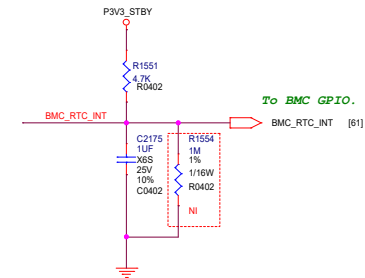
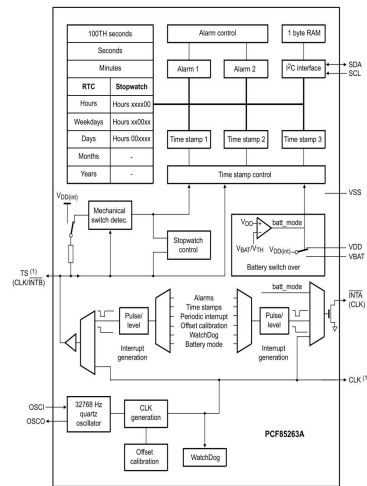
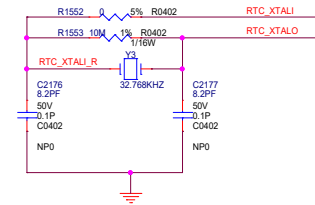
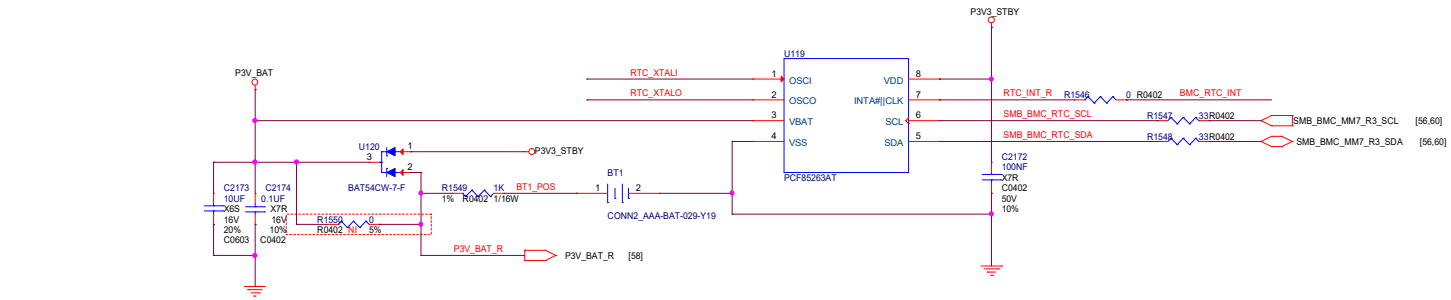


FUNCTION TABLE
(each multiplexer/demultiplexer)

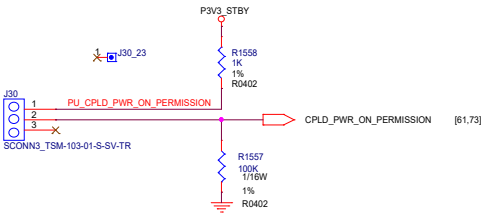
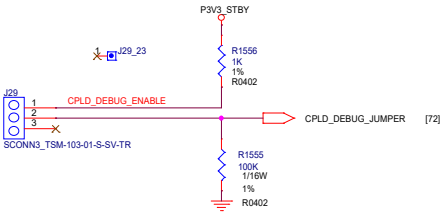
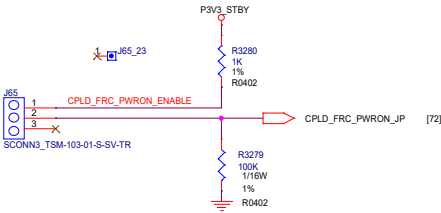
INPUTS			FUNCTION
OE	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

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I2C_RTC_IC

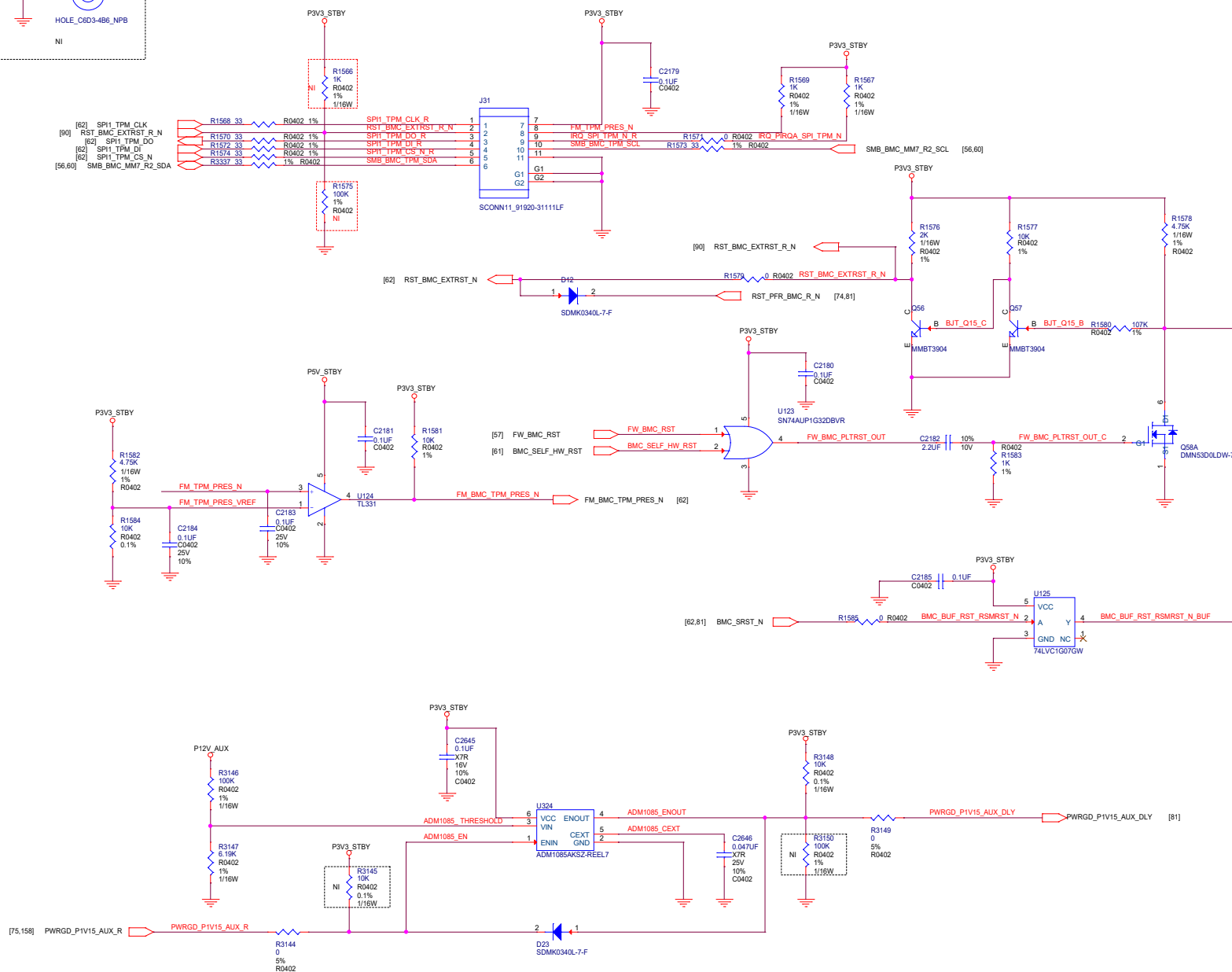


CPLD FORCE PWRON HEADER

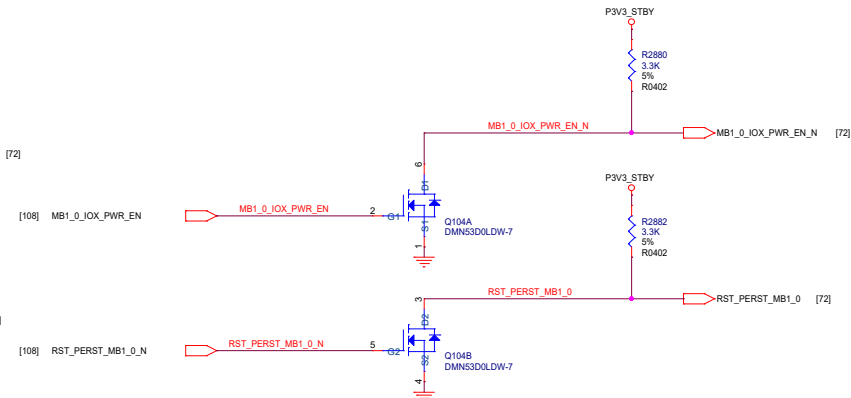
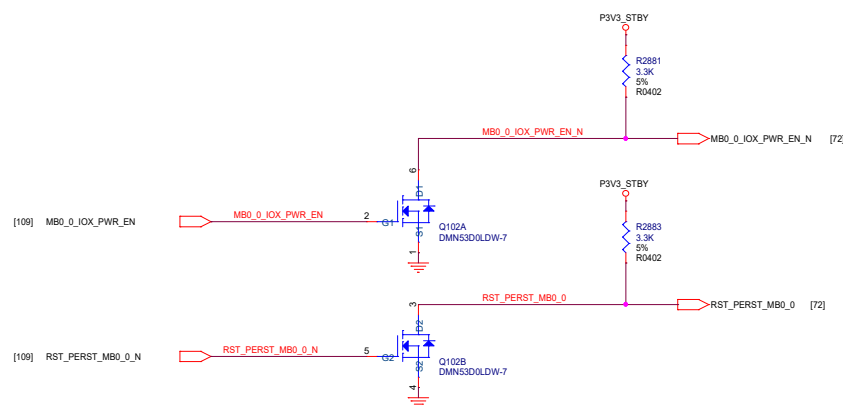
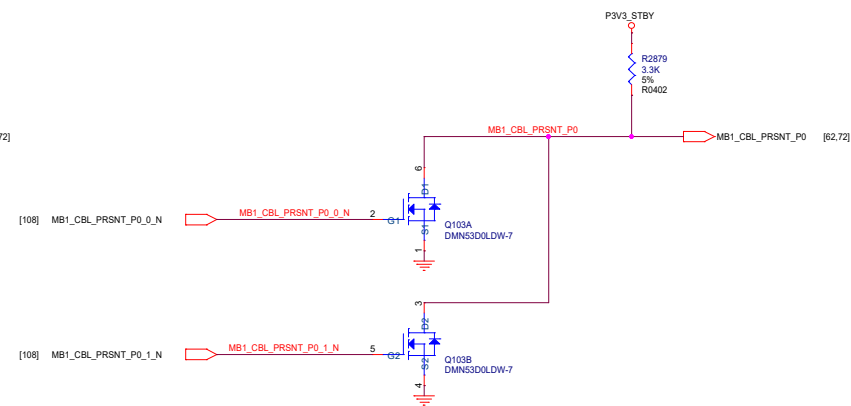
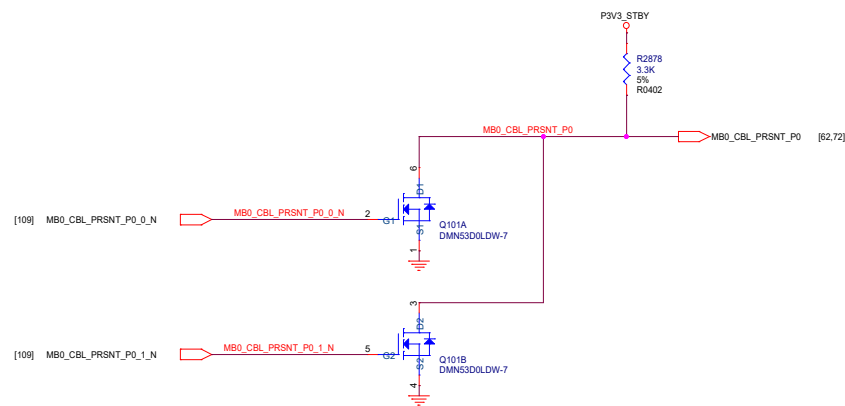


BMC&CPLD DEBUG HEADER

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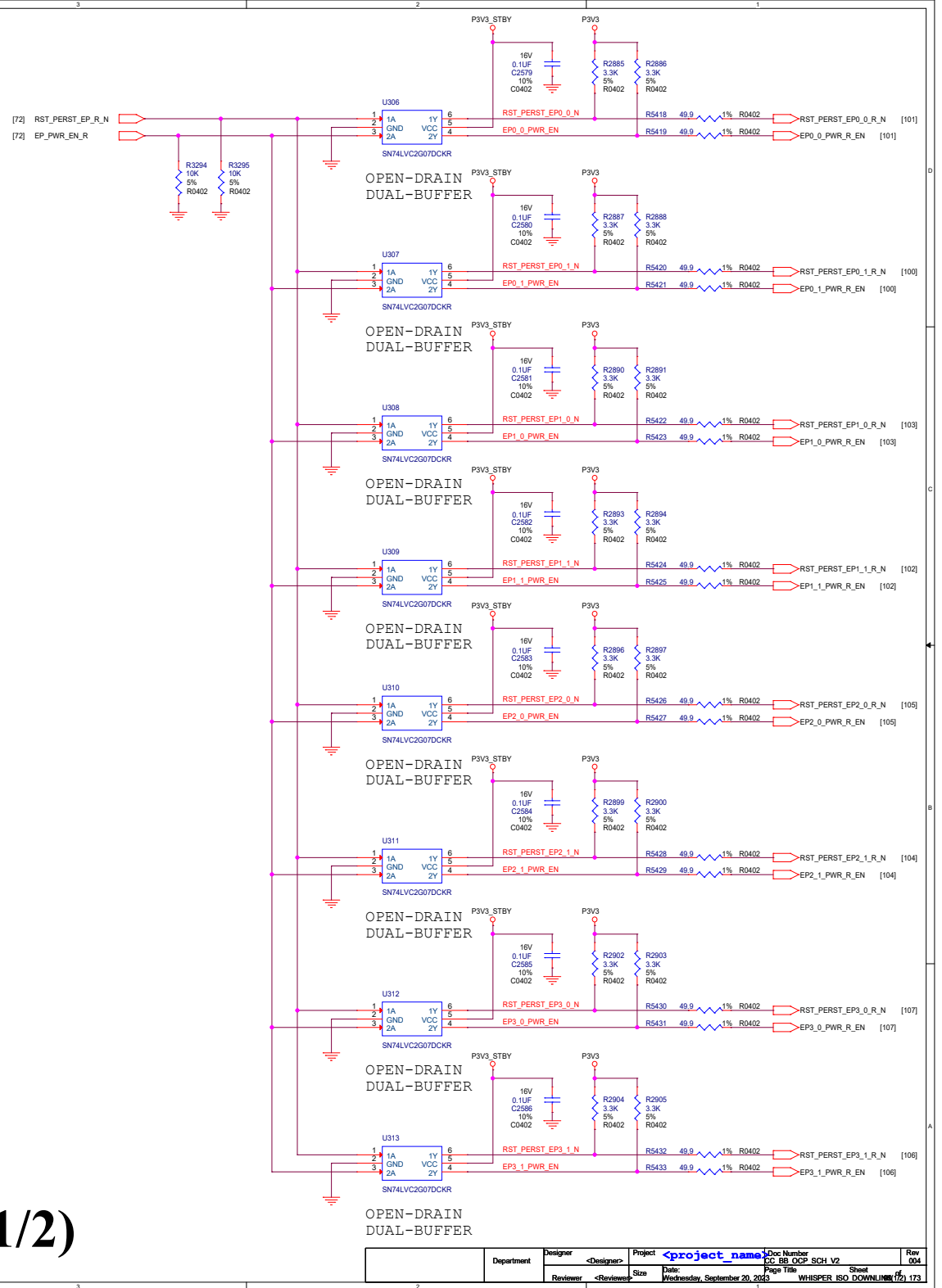


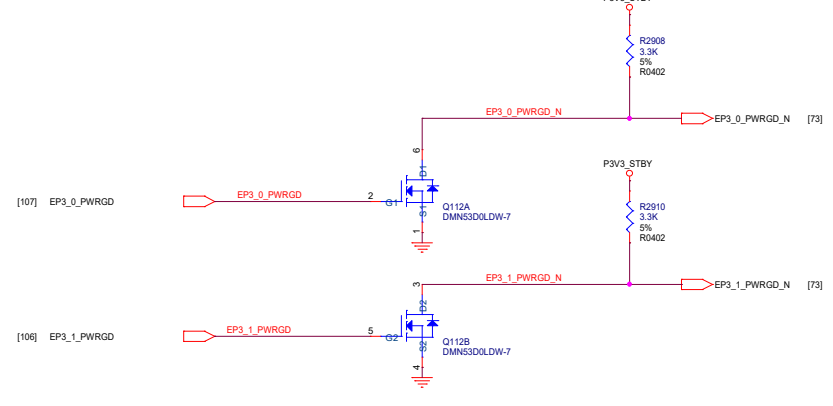
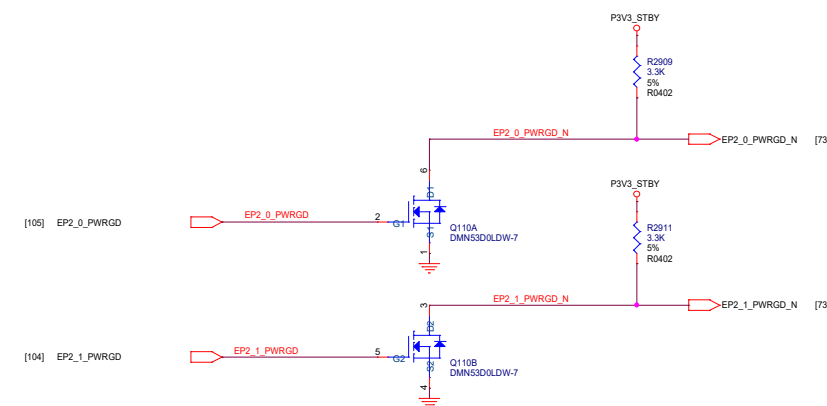
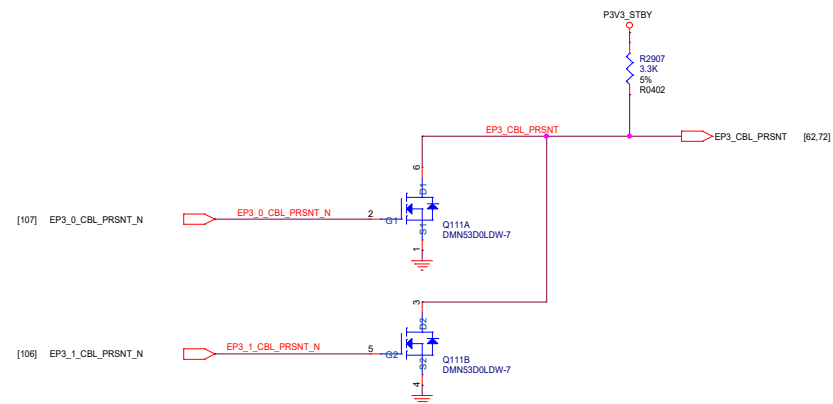
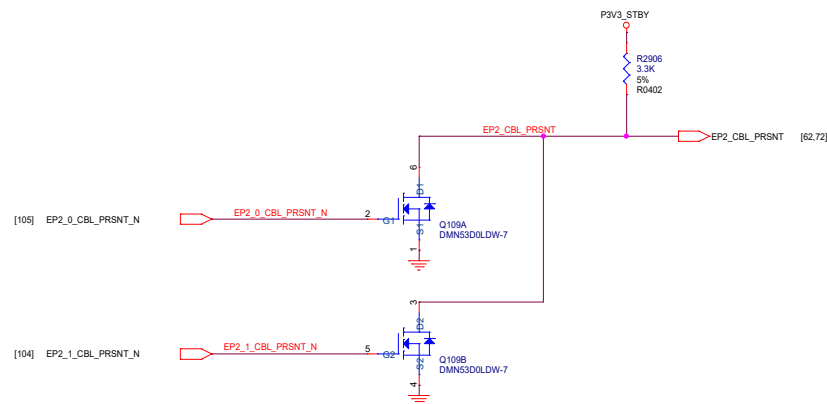
TPM CONN



WHISPER_ISO_UPLINK(2/2)

WHISPER_ISO_DOWNLINK(1/2)





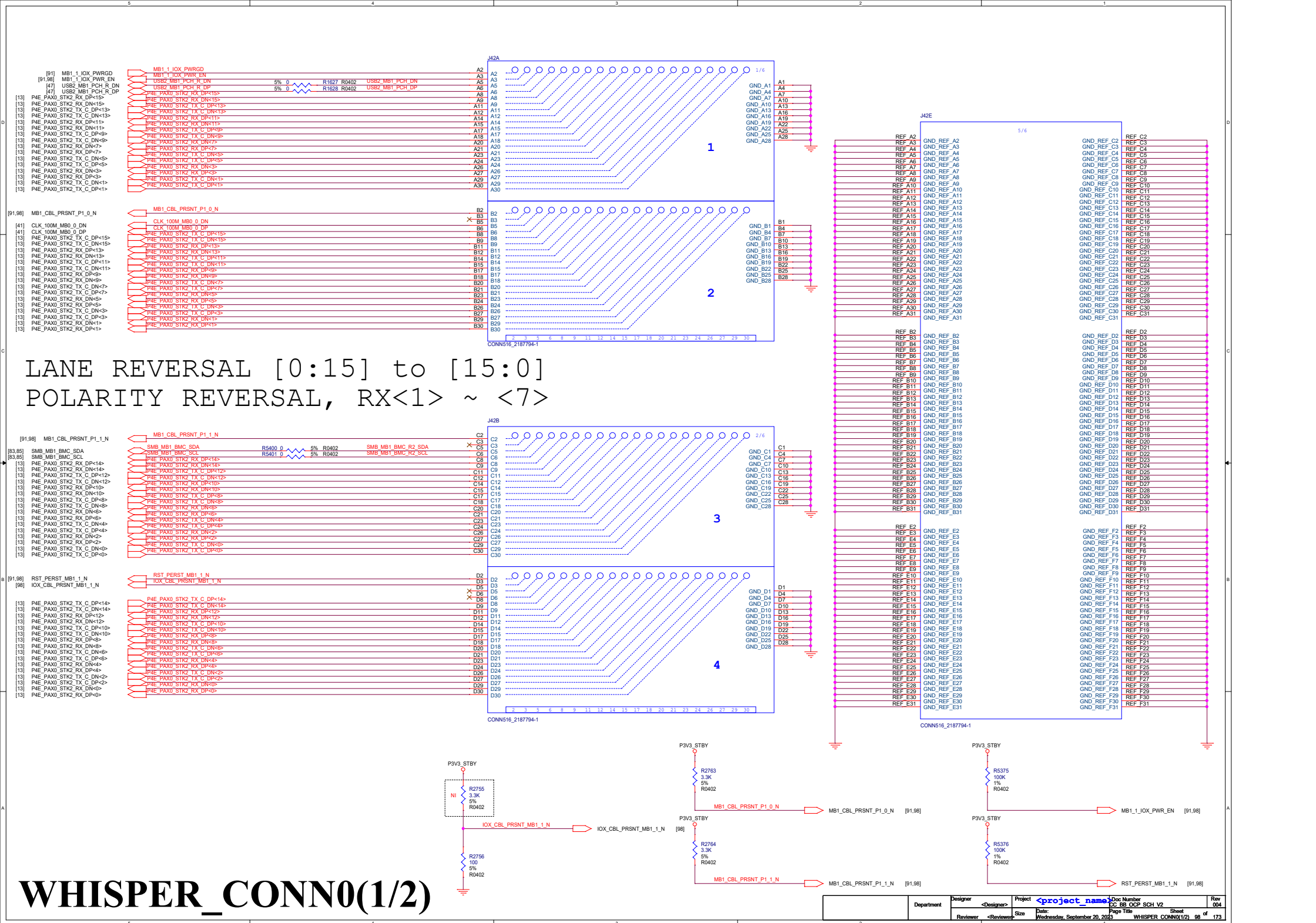
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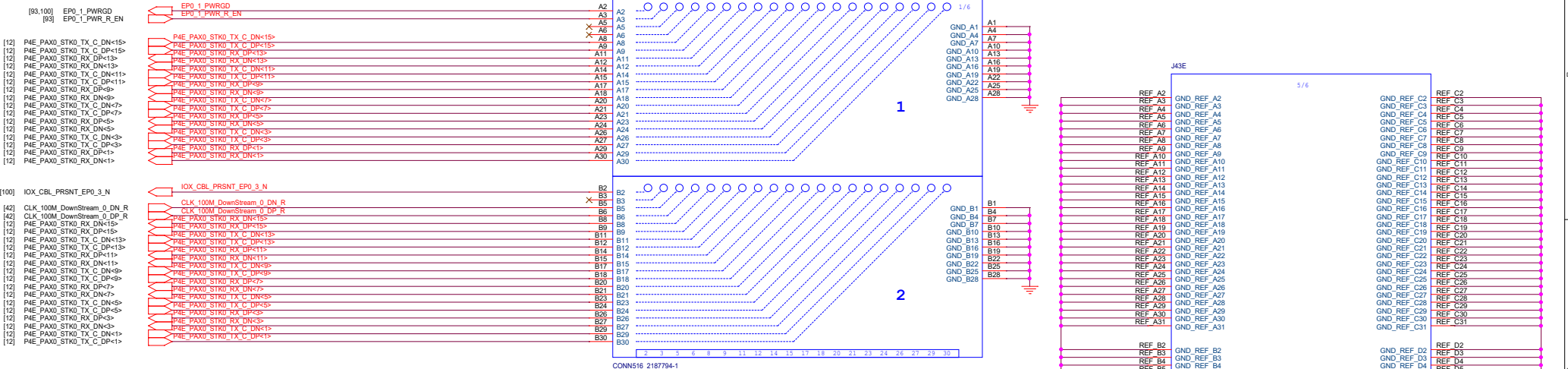
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	<Designer>	<project_name>	CC-BB-DCP-SCH-V2	004
Reviewer	<Reviewer>	Date:	Page Title	Sheet
		Wednesday, September 20, 2023	WHISPER ISO DOWNLINK	173

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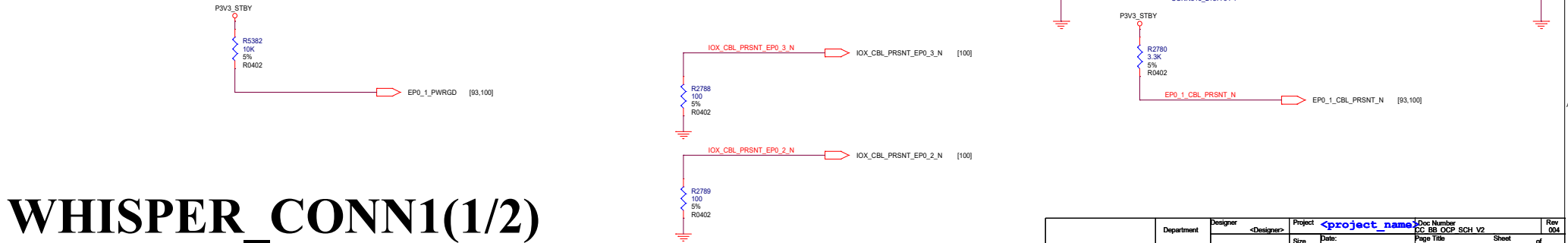
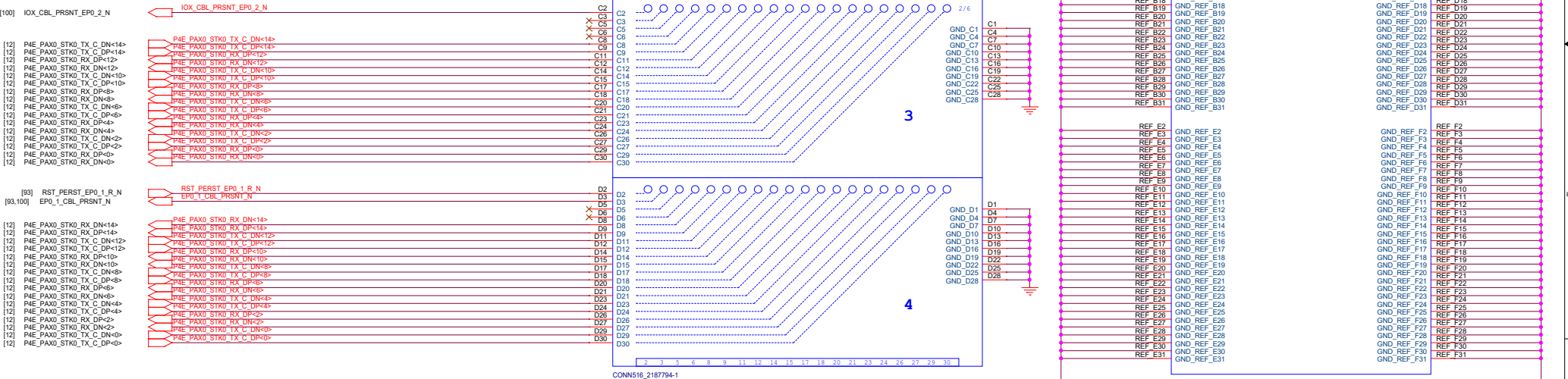
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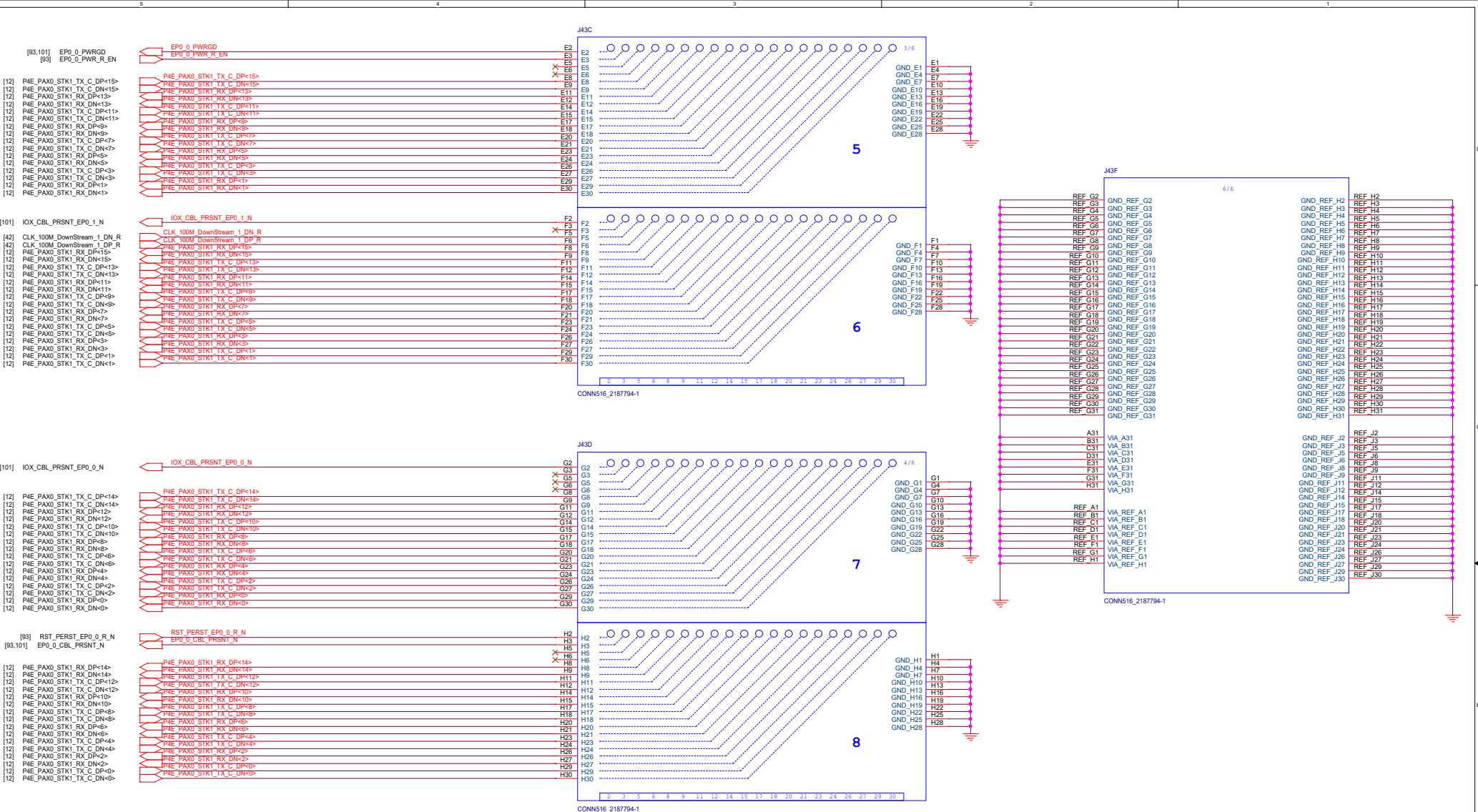




LANE REVERSAL [0:15] to [15:0]
POLARITY REVERSAL, TX<0>~<15>, RX<14>~<15>

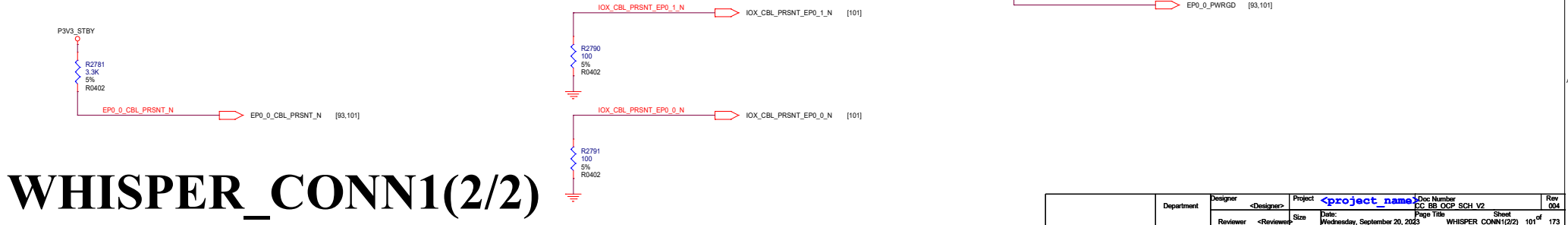


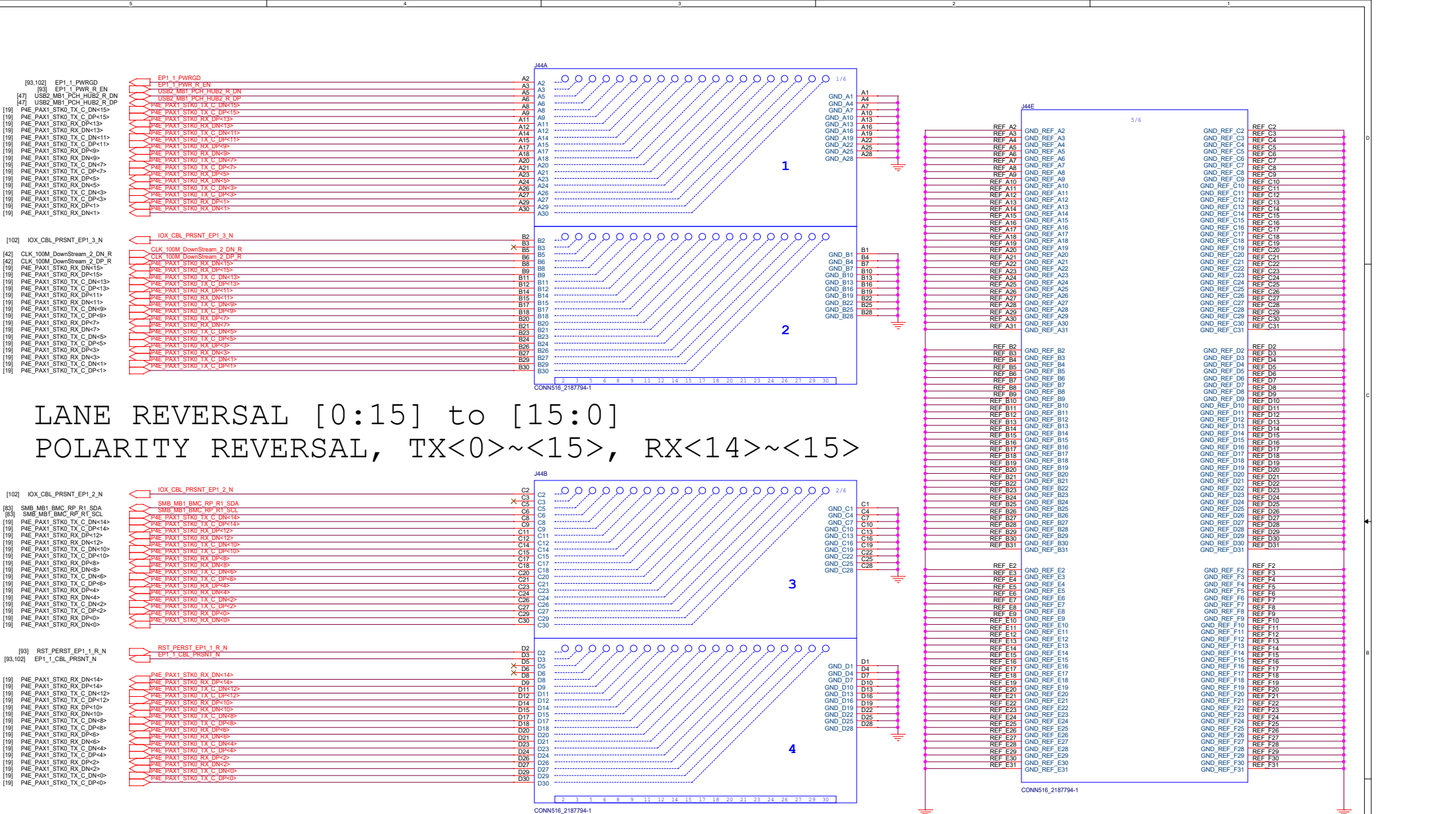
WHISPER_CONN1(1/2)



LANE REVERSAL [0:15] to [15:0]
POLARITY REVERSAL TX<15>

WHISPER_CONN1(2/2)

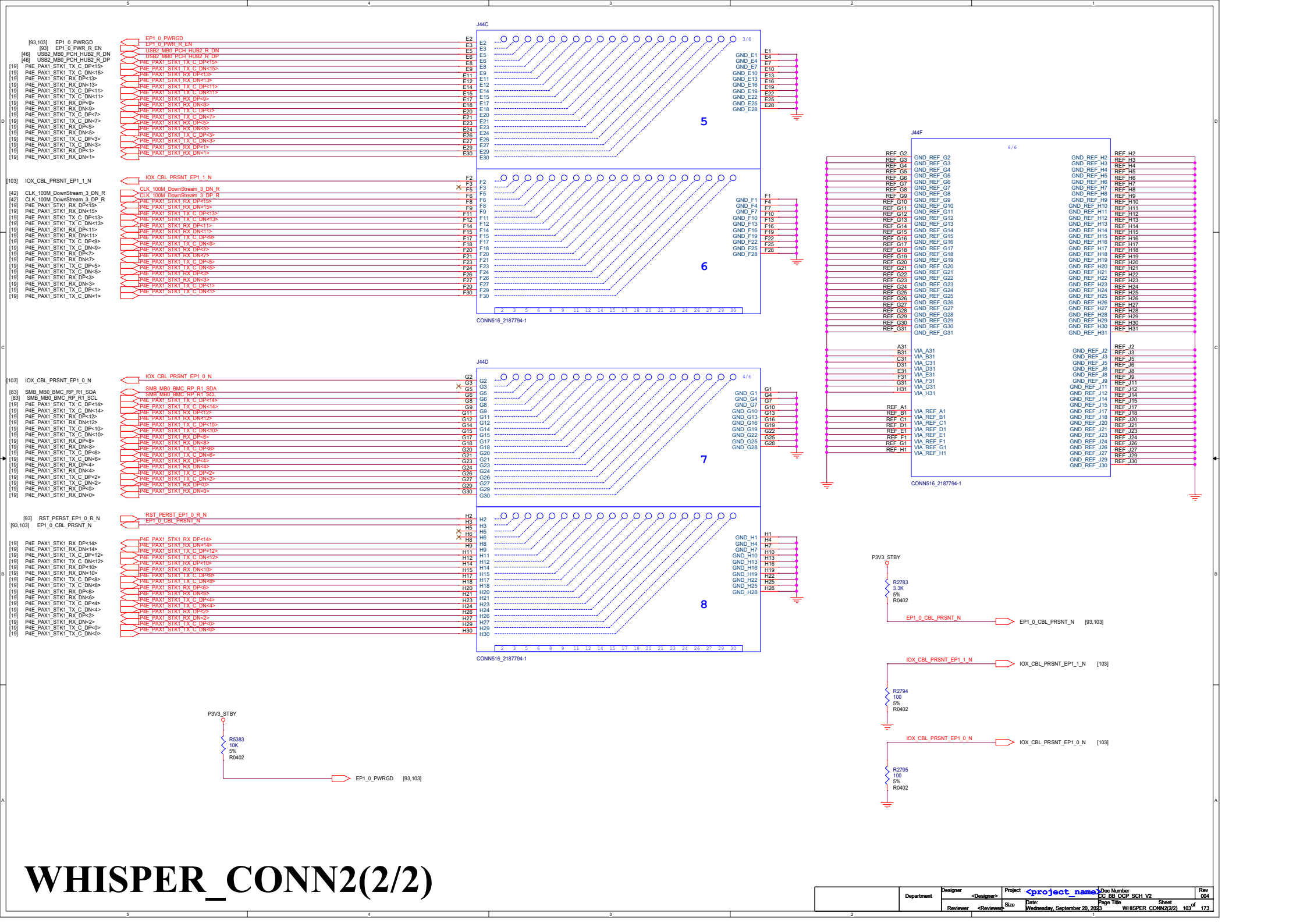




LANE REVERSAL [0:15] to [15:0]
POLARITY REVERSAL, TX<0>~<15>, RX<14>~<15>

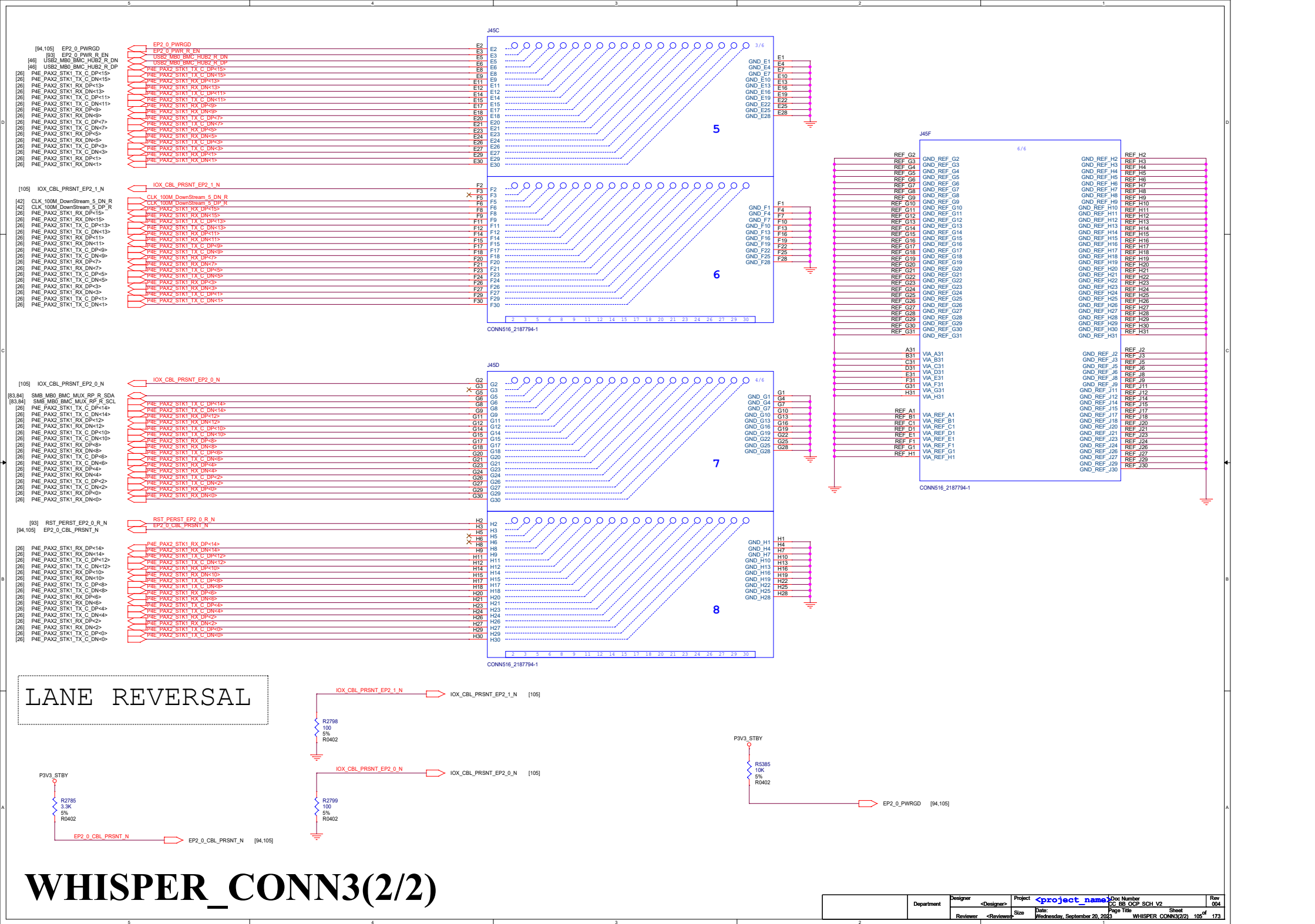


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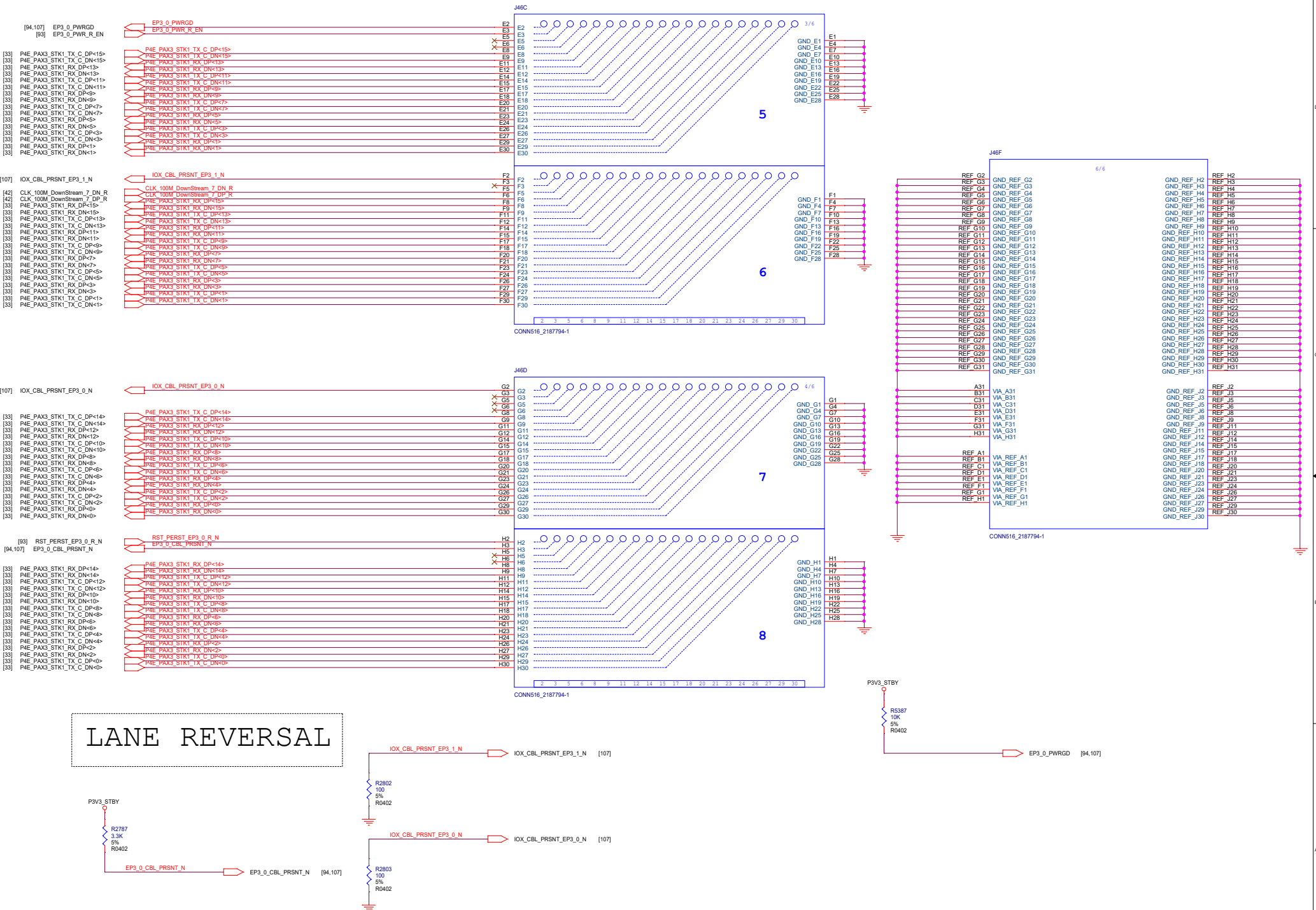
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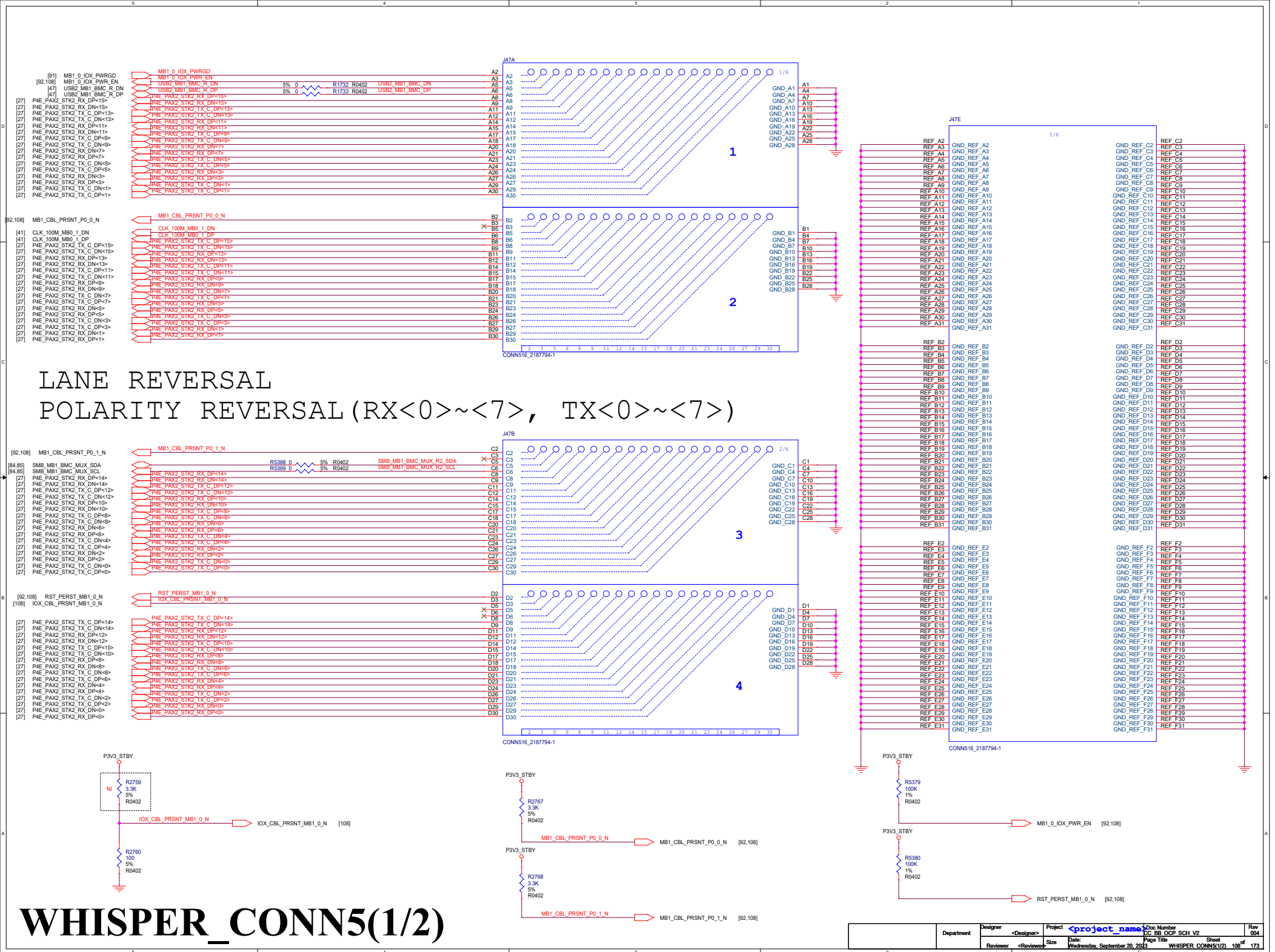
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Reviewer	<Reviewer>	Date	Page Title	Sheet
		Wednesday, September 20, 2023	WHISPER_CONN2(2/2)	103 of 173

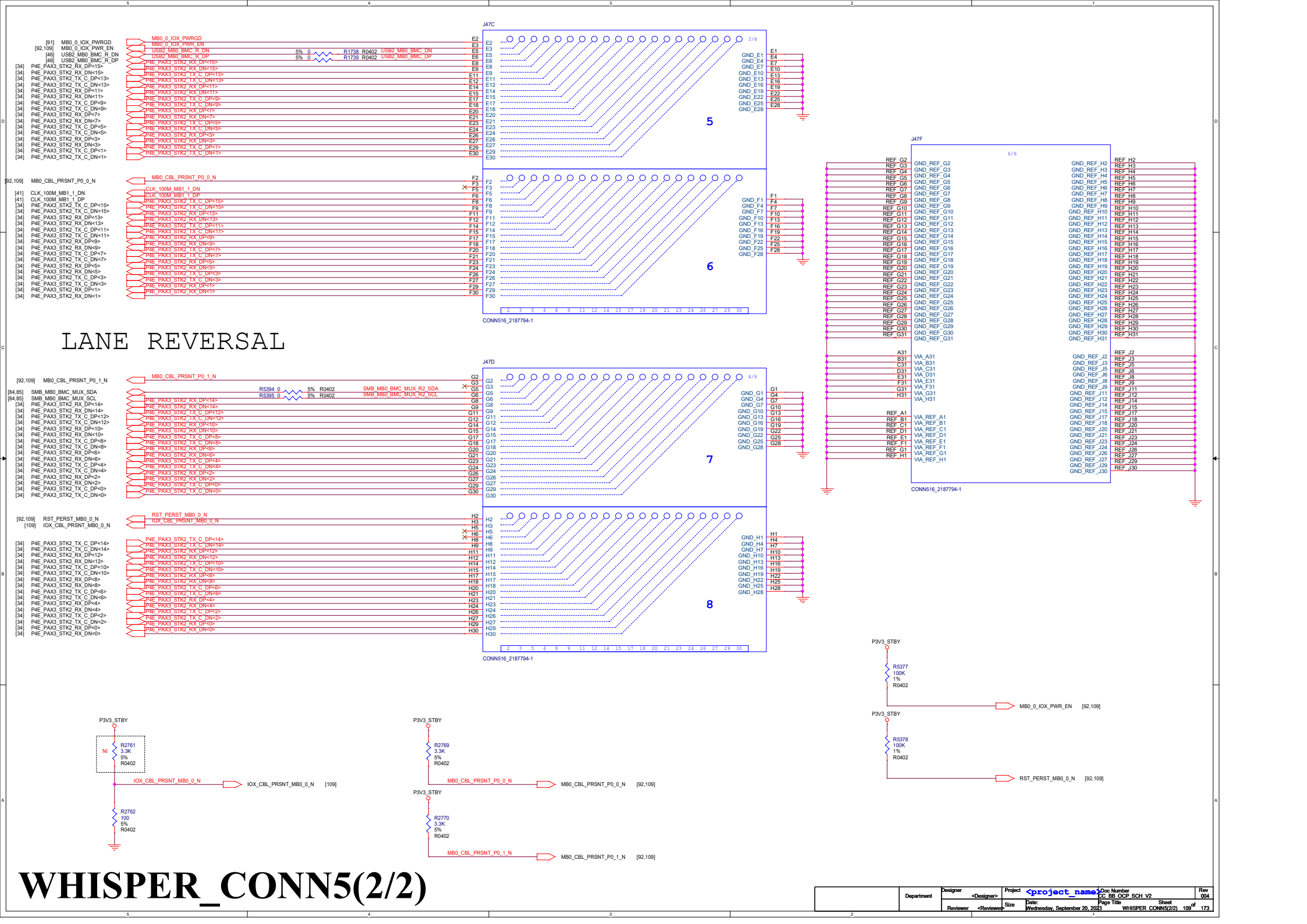


WHISPER_CONN4(2/2)

LANE REVERSAL



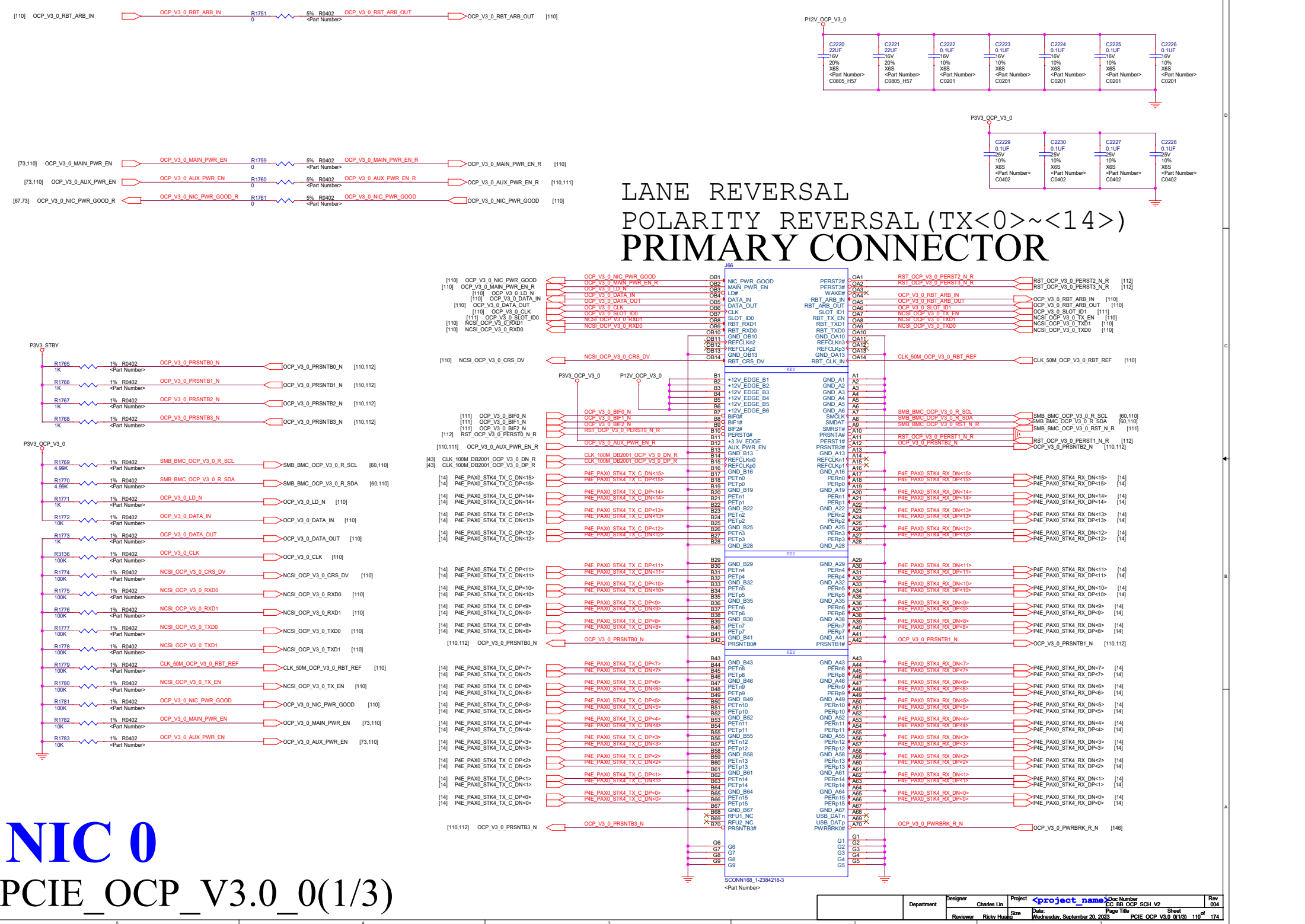


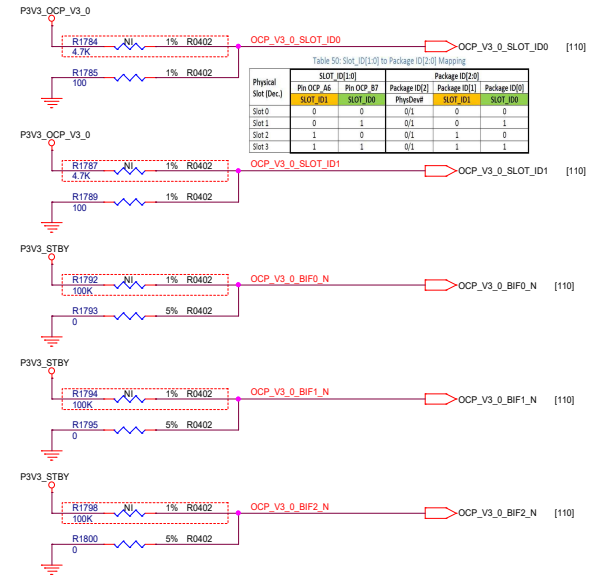
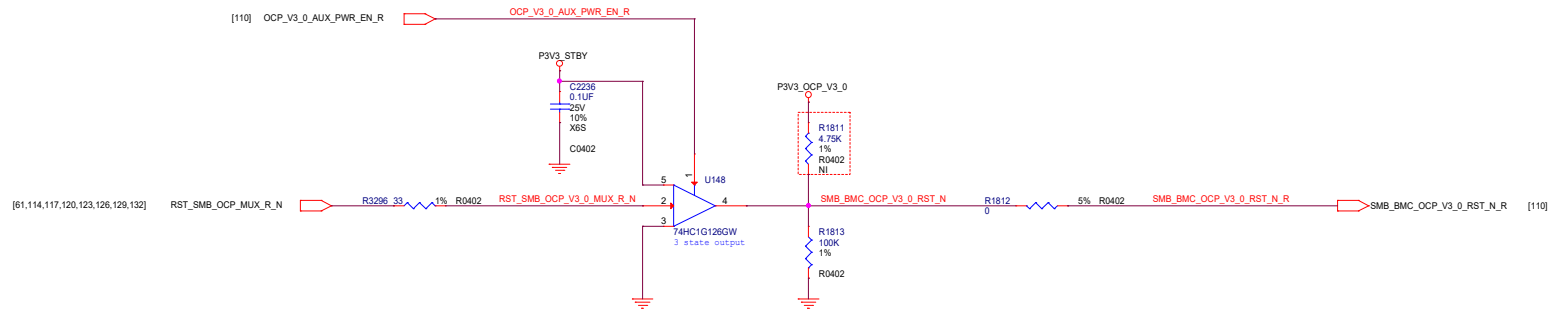


NIC 0

PCIE_OCP_V3.0_0(1/3)

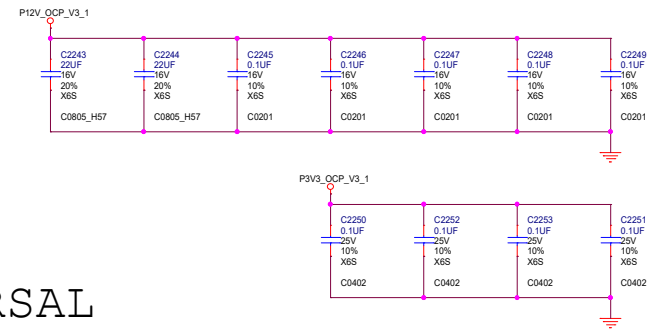
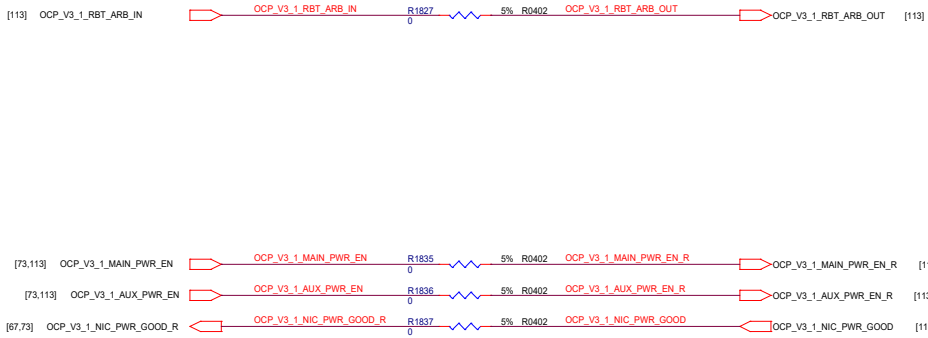
LANE REVERSAL
POLARITY REVERSAL (TX<0>~<14>)
PRIMARY CONNECTOR



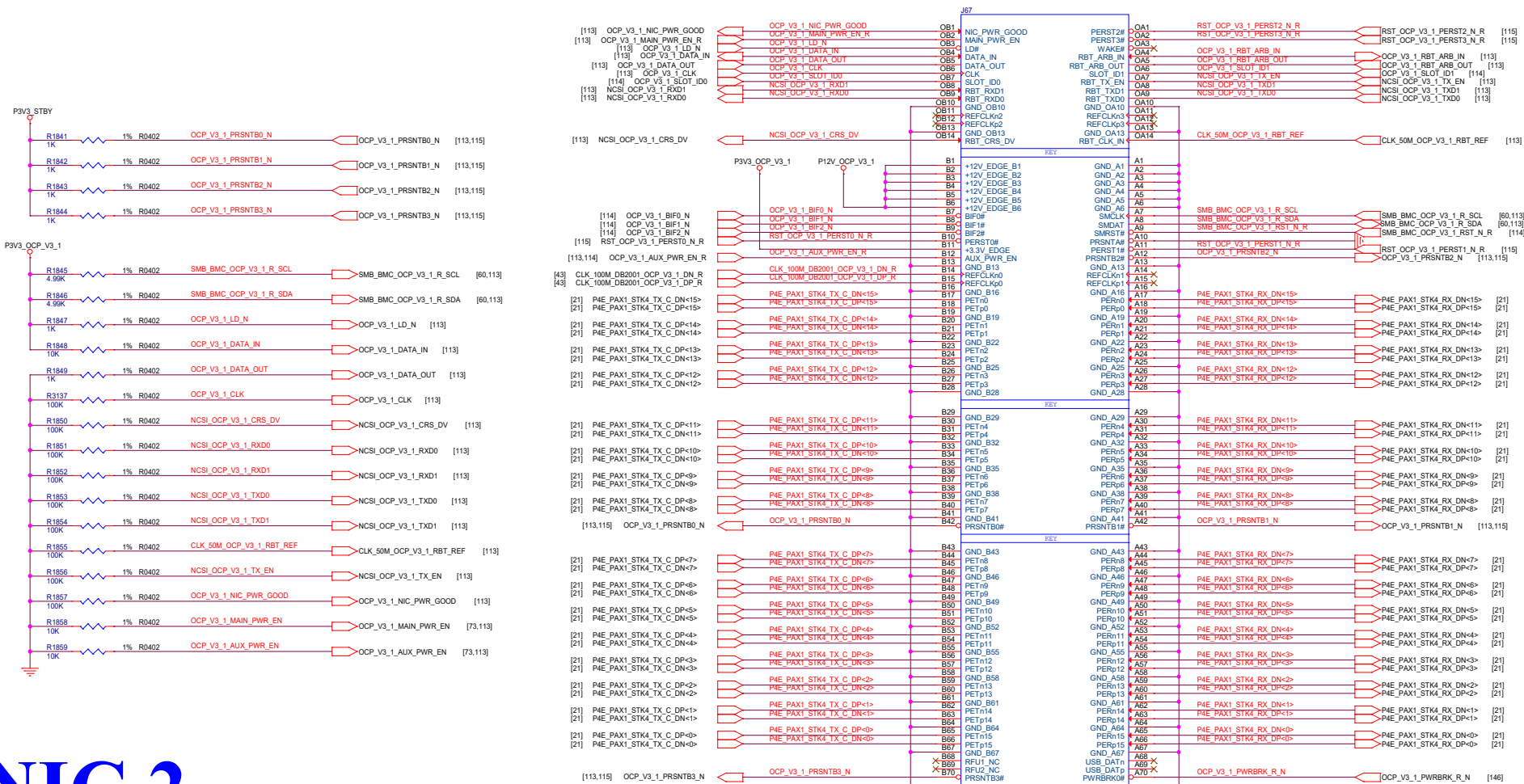


PCIE_OCP_V3.0_0(3/3)

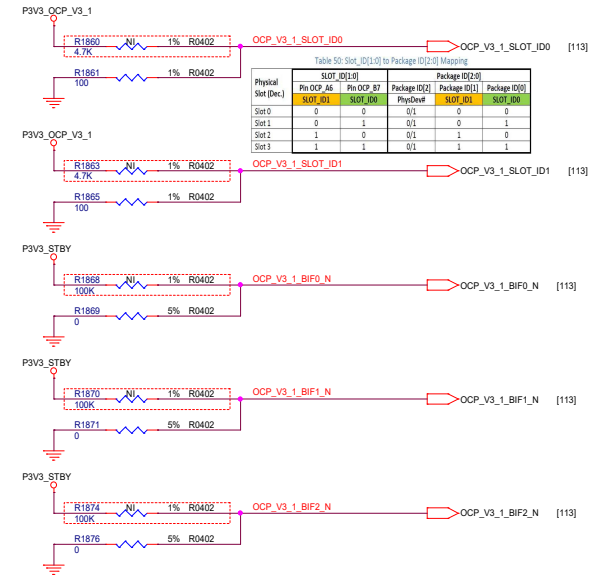
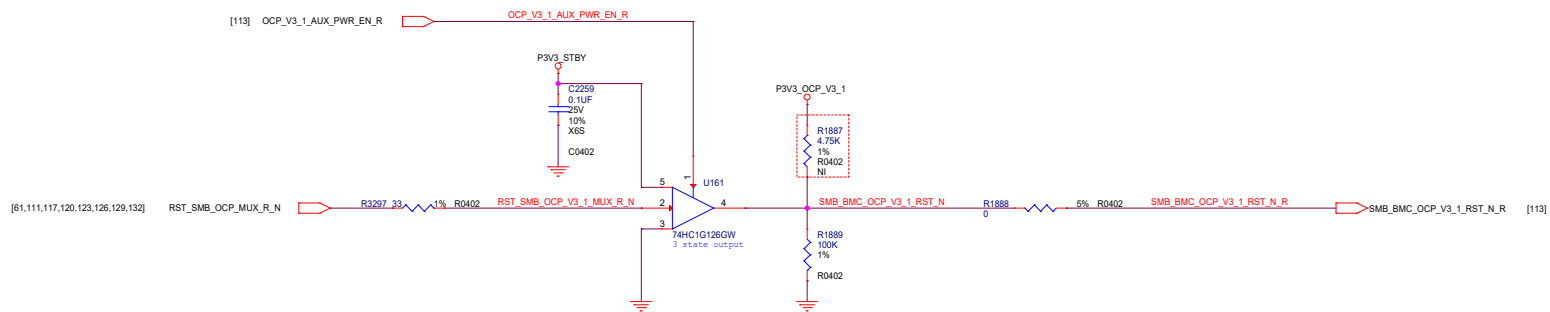


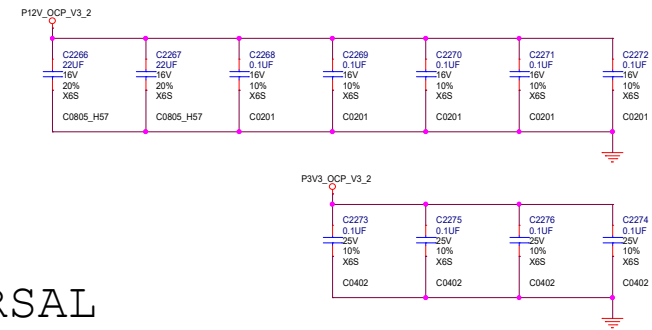


LANE REVERSAL POLARITY REVERSAL (TX<0>~<14>) PRIMARY CONNECTOR



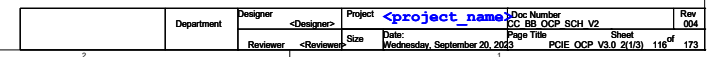
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PCIE_OCP_V3.0_1(1/3)

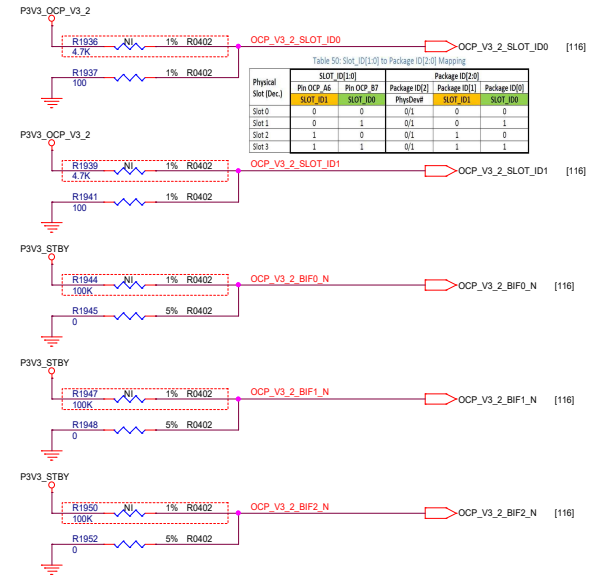
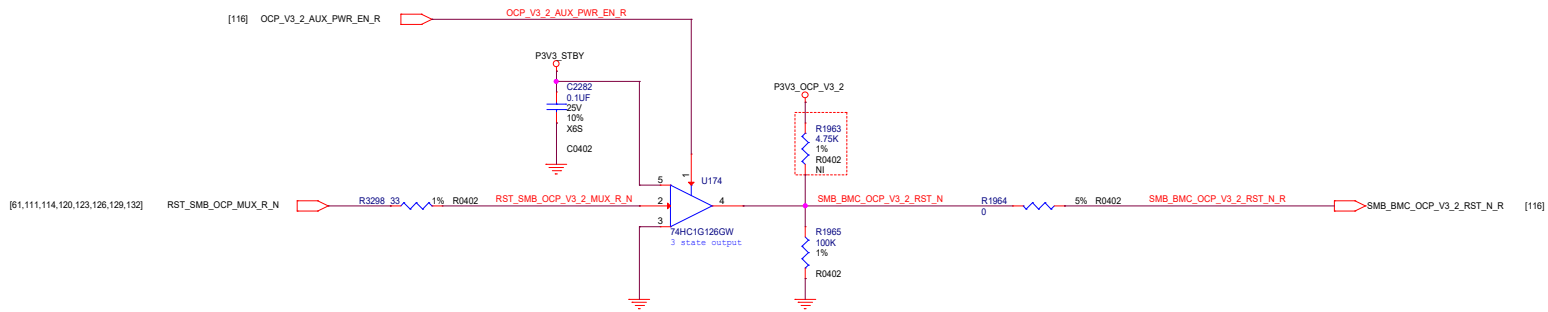




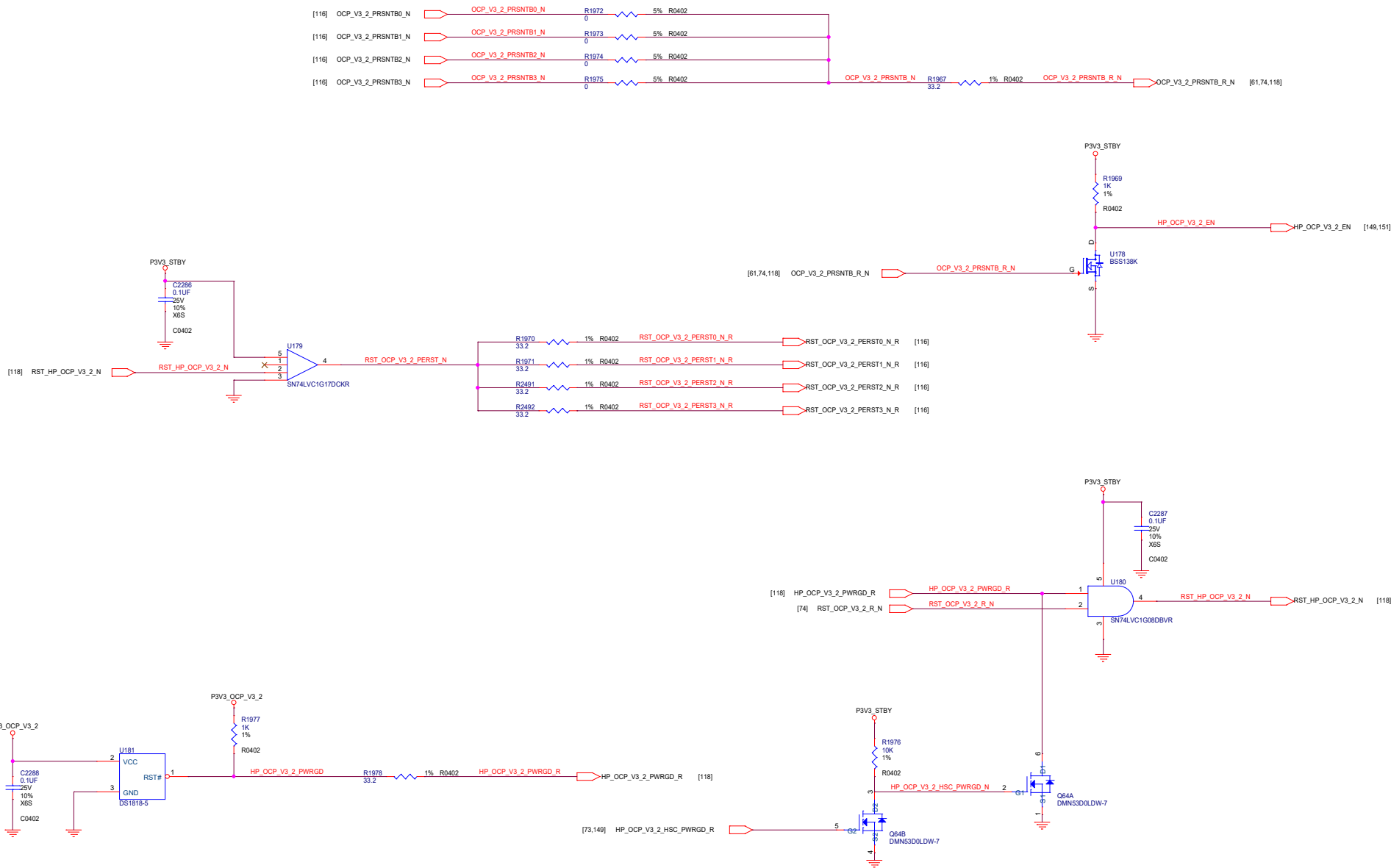
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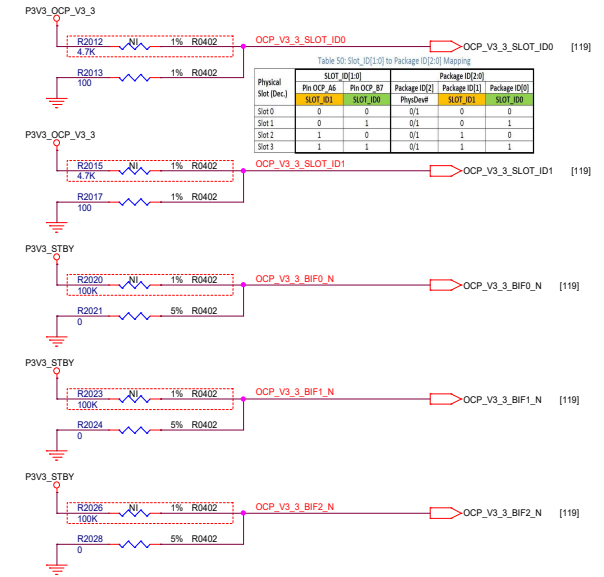
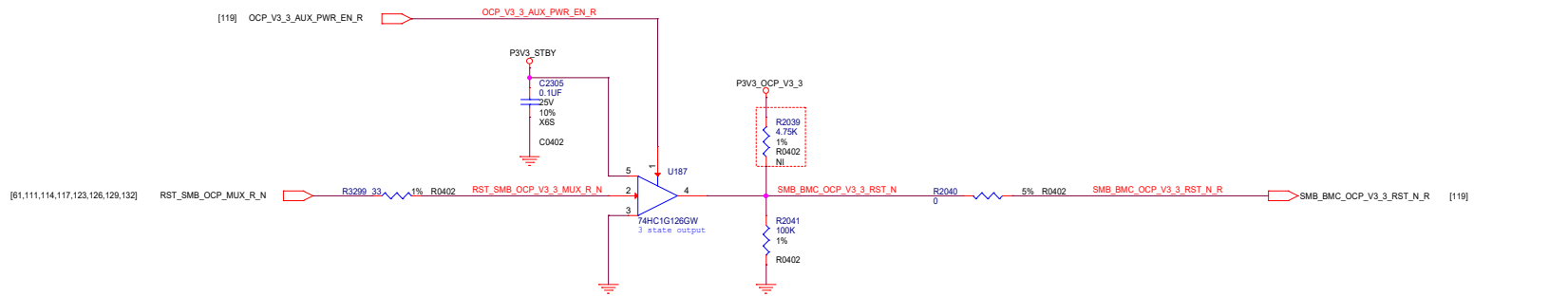
PCIE_OCP_V3.0_2(1/3)





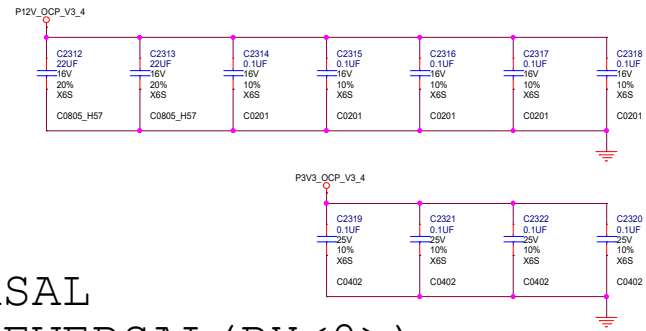
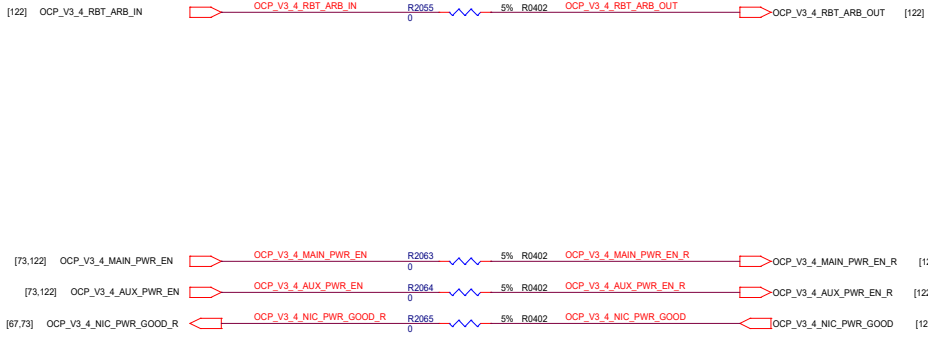
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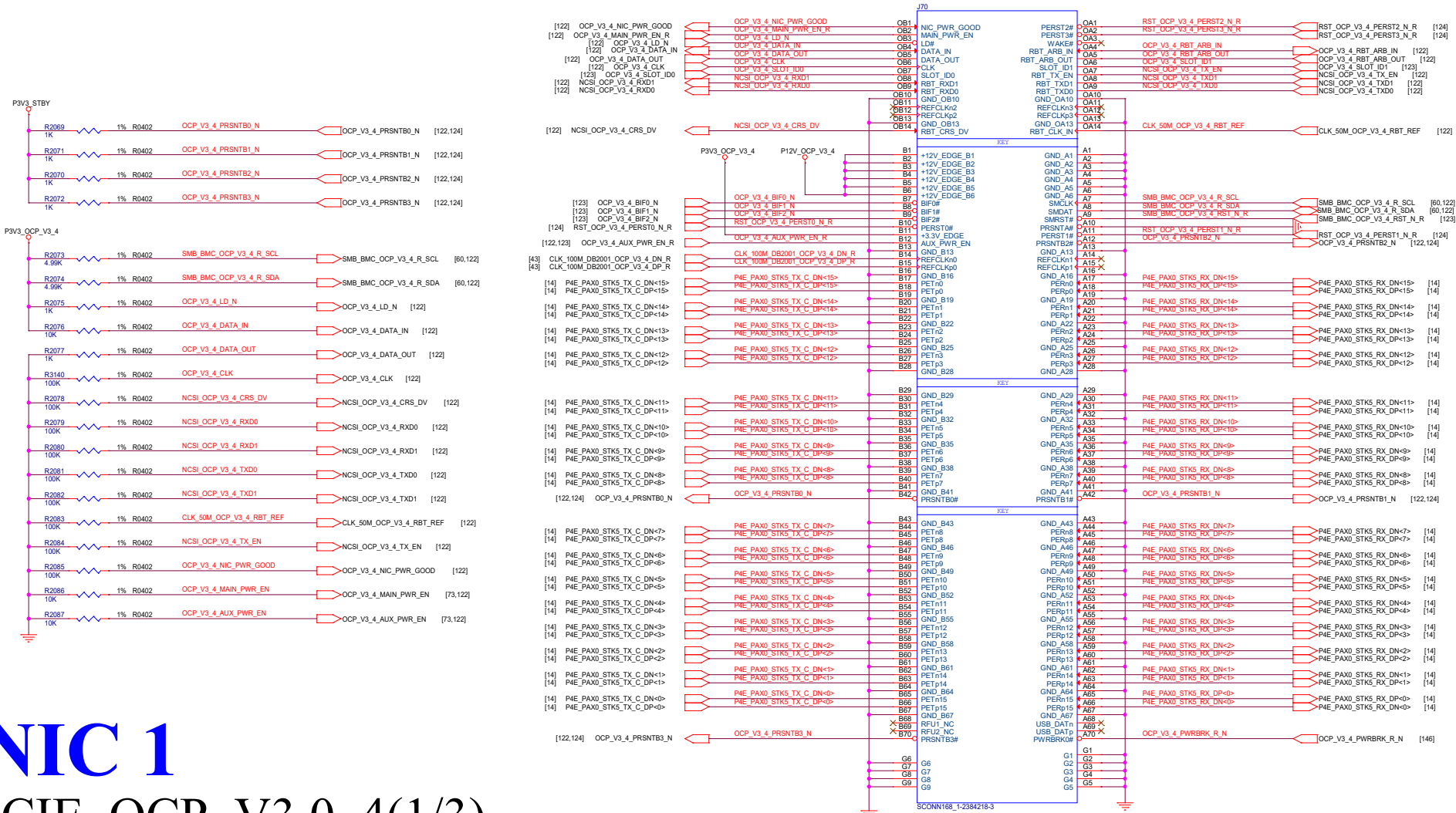


PCIE_OCP_V3.0_3(3/3)

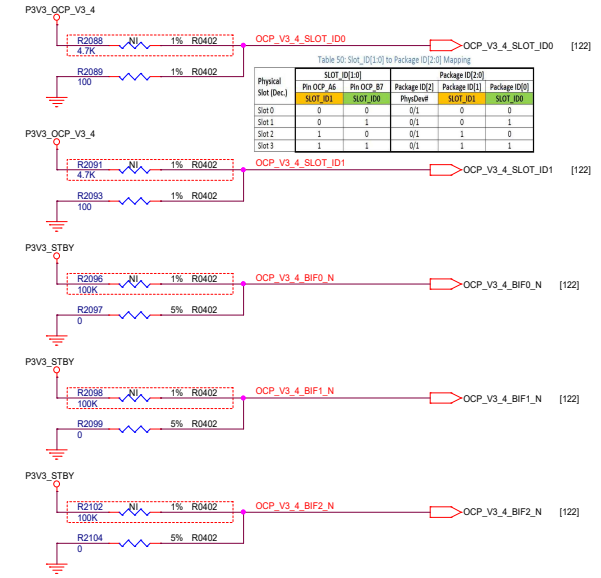
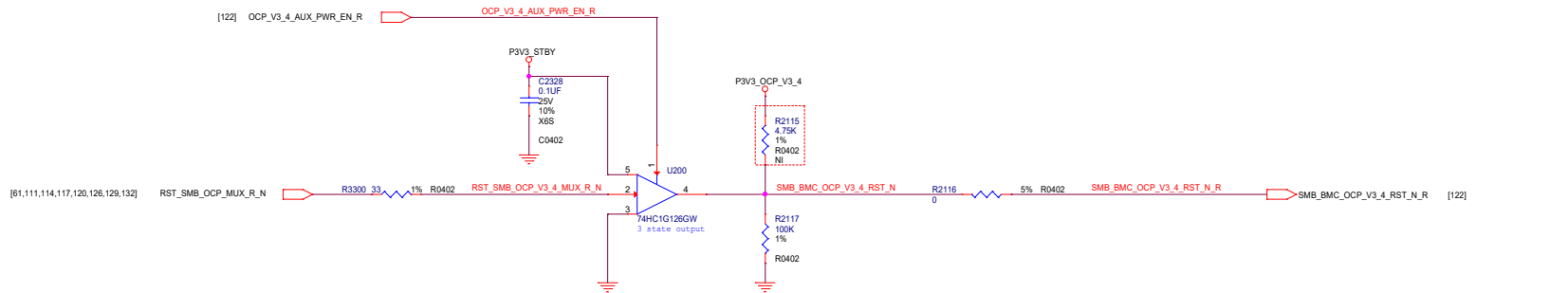




LANE REVERSAL POLARITY REVERSAL (RX<0>) PRIMARY CONNECTOR

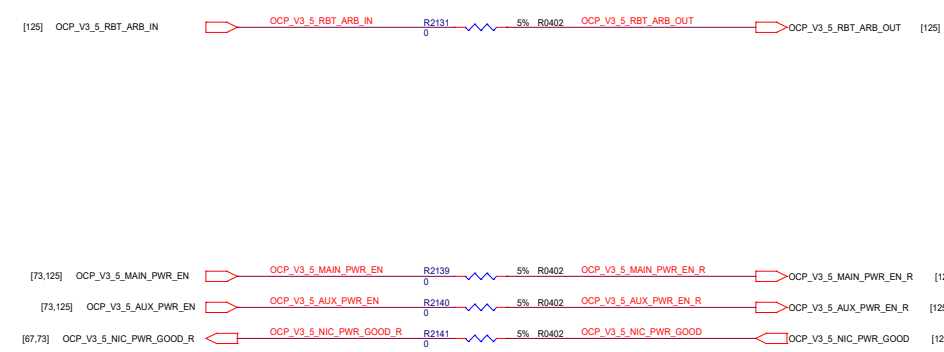


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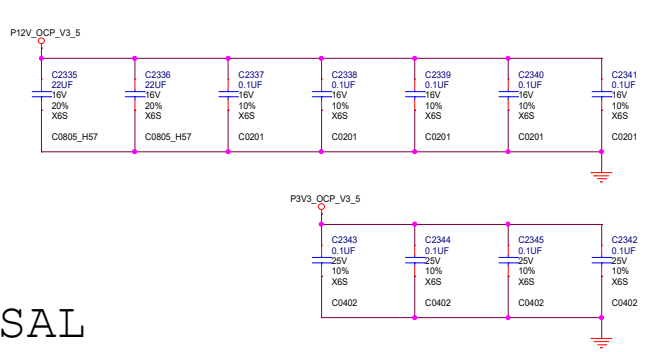


PCIE_OCP_V3.0_4(3/3)

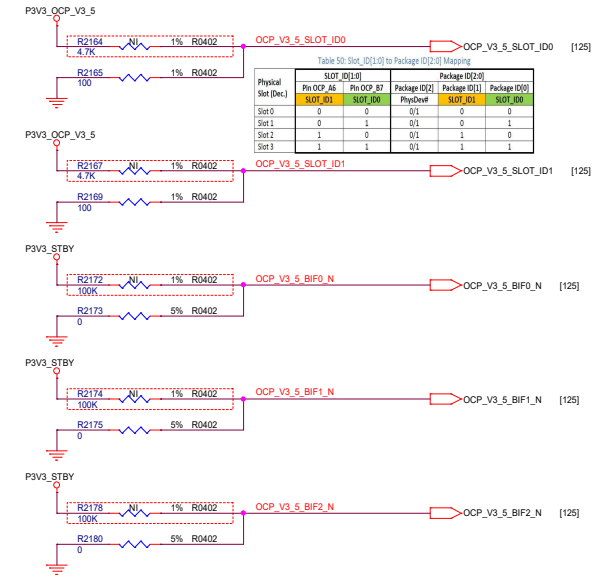
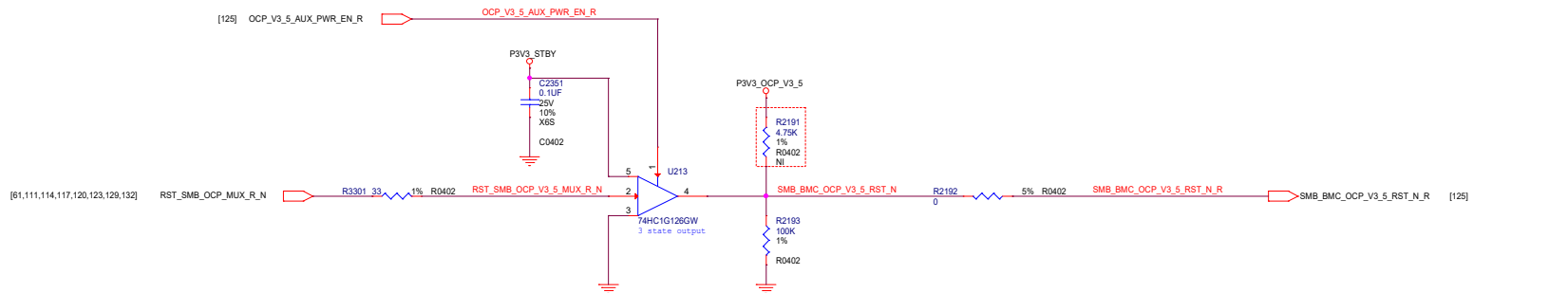


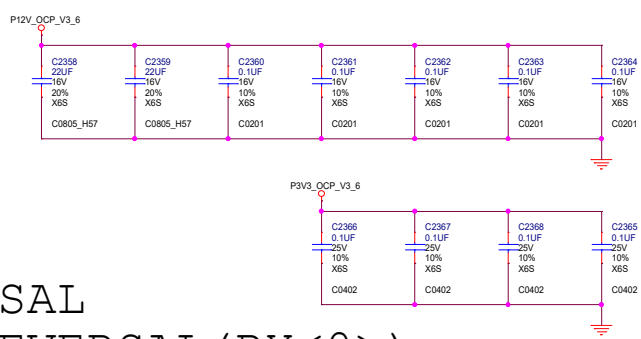
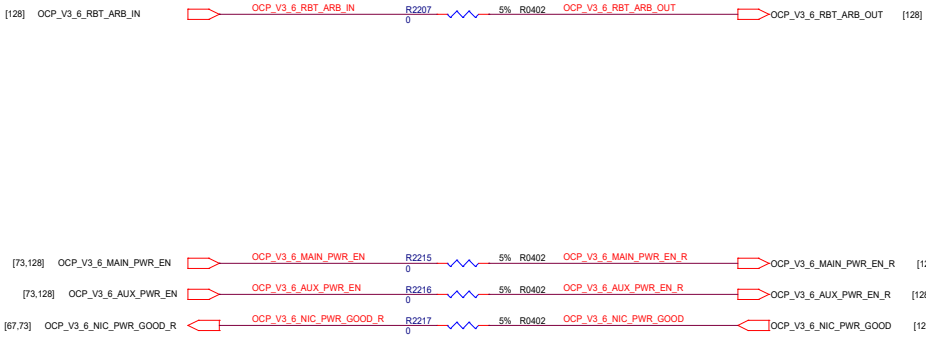


LANE REVERSAL POLARITY REVERSAL (RX<0>) PRIMARY CONNECTOR

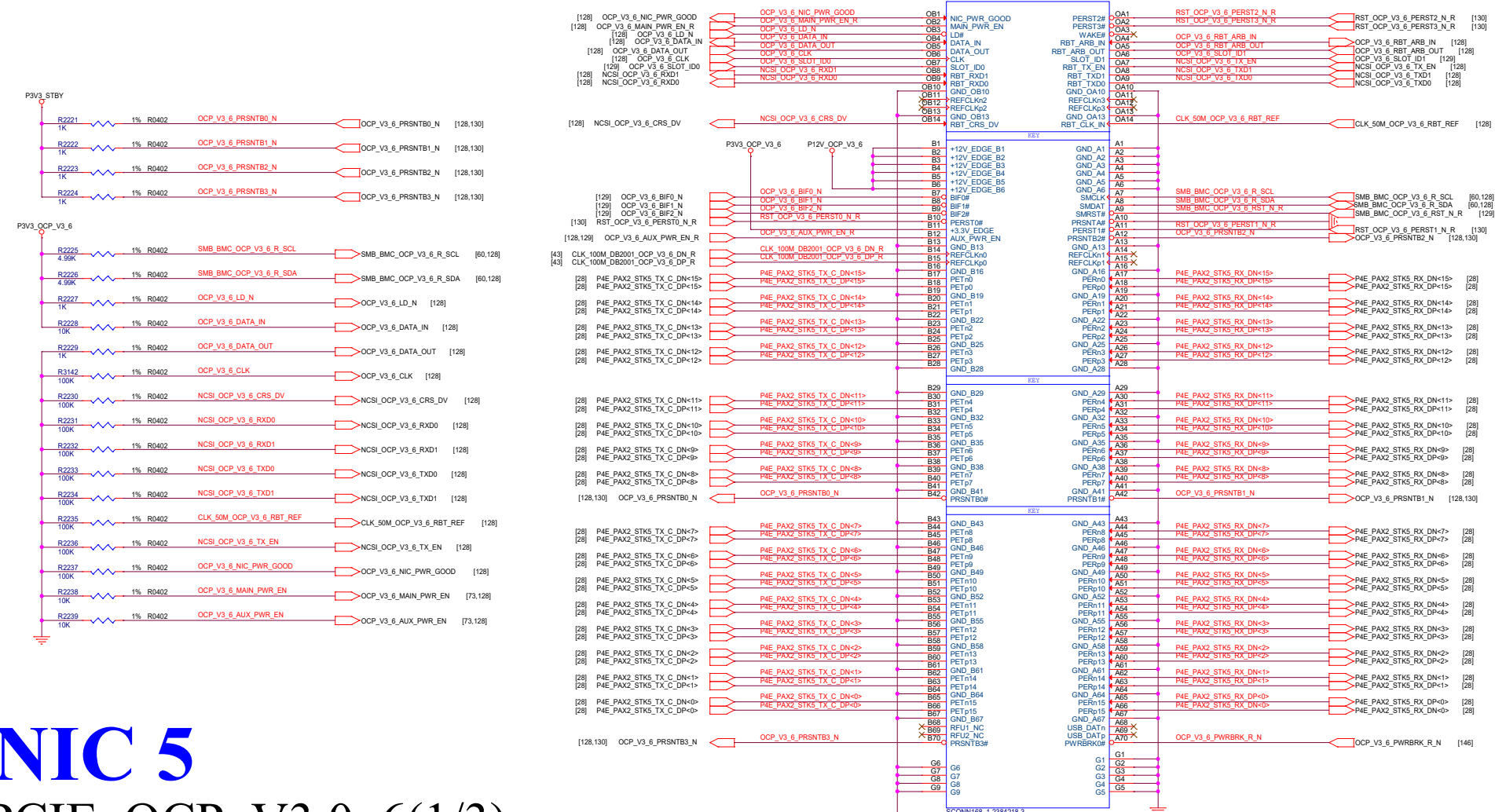


NIC 3
PCIE_OCP_V3.0_5(1/3)

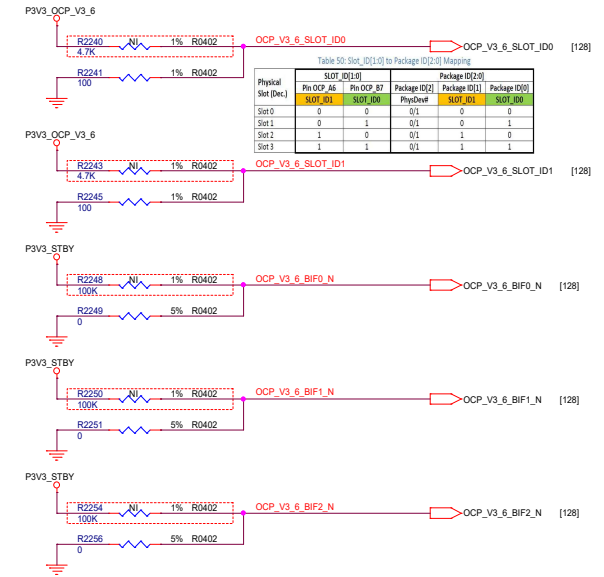
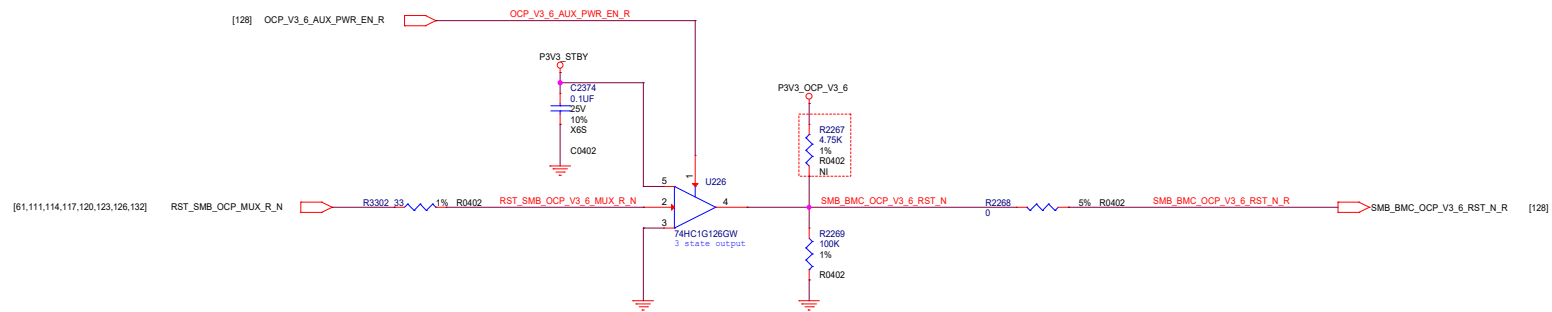




LANE REVERSAL POLARITY REVERSAL (RX<0>) PRIMARY CONNECTOR

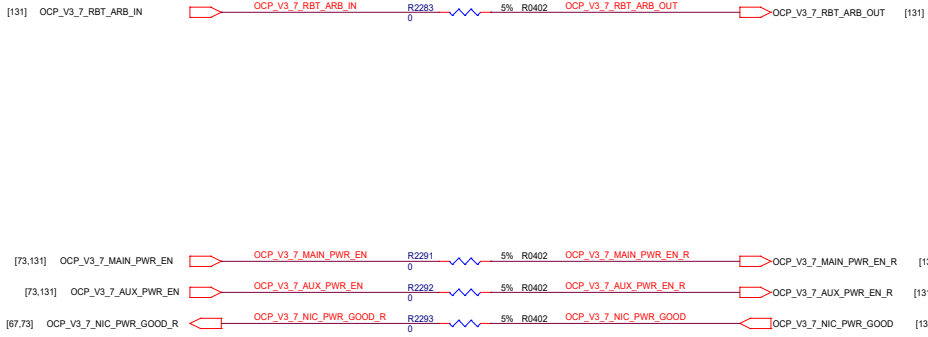


NIC 5
PCIE_OCP_V3.0_6(1/3)

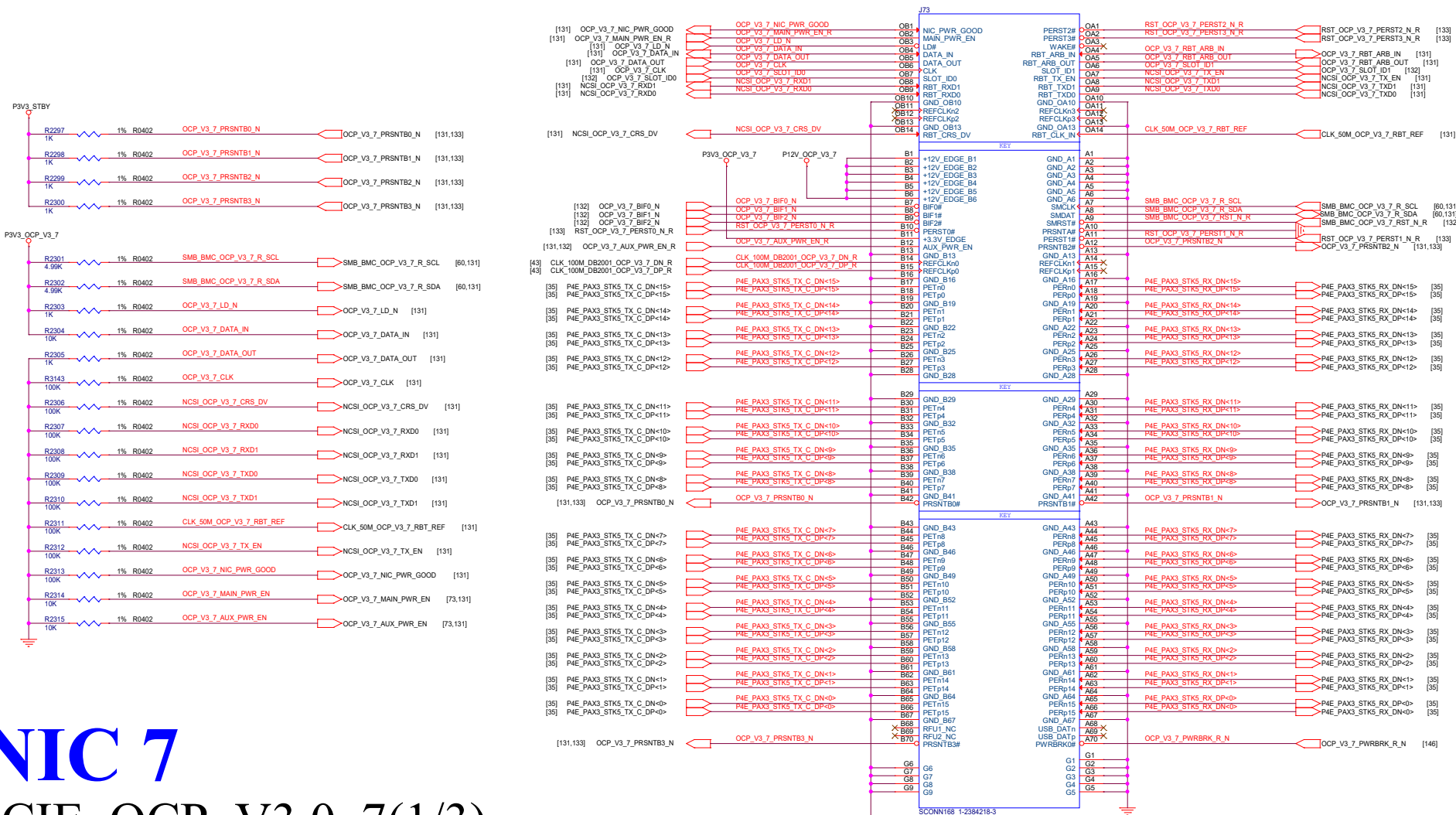
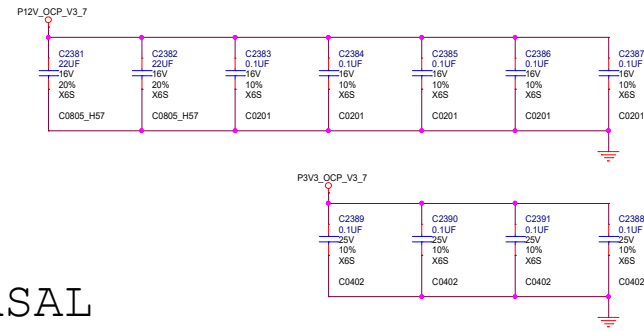


PCIE_OCP_V3.0_6(3/3)

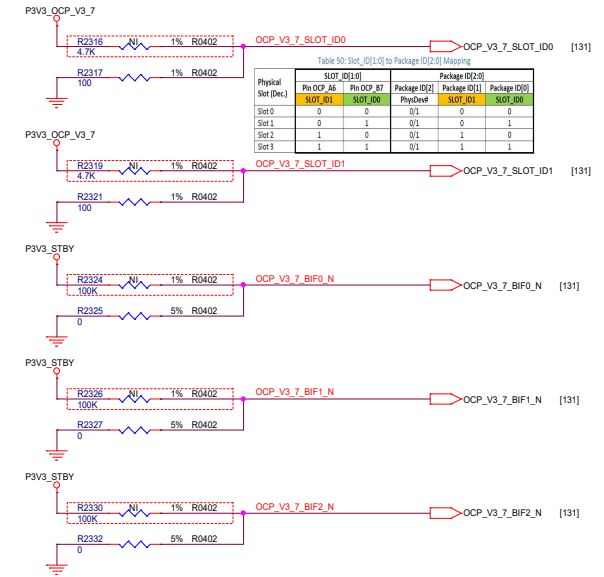
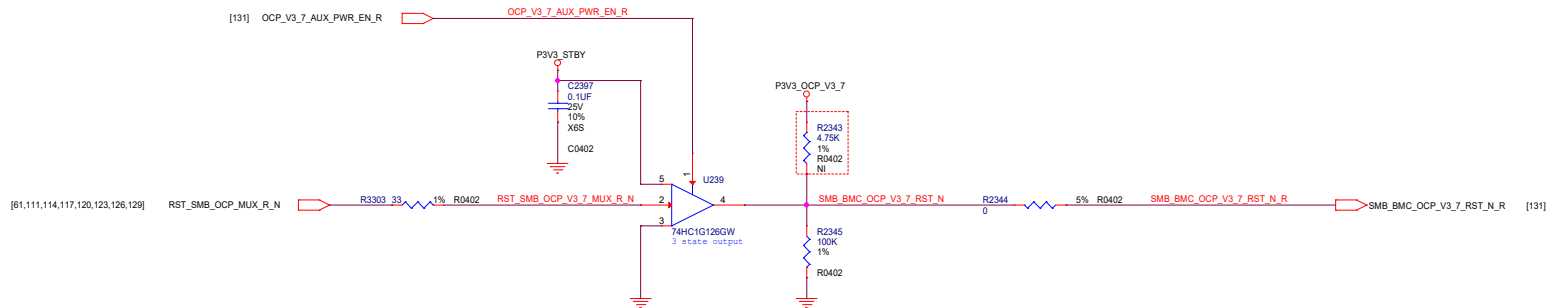




LANE REVERSAL POLARITY REVERSAL (RX<0>) PRIMARY CONNECTOR



NIC 7
PCIE_OCP_V3.0_7(1/3)

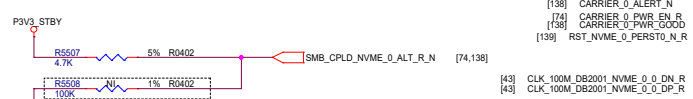
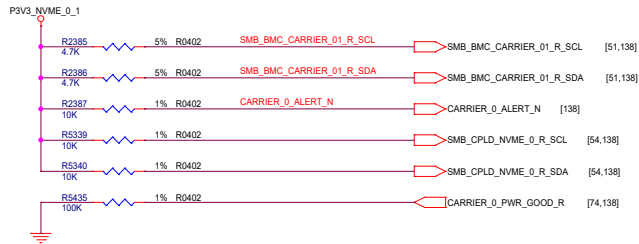
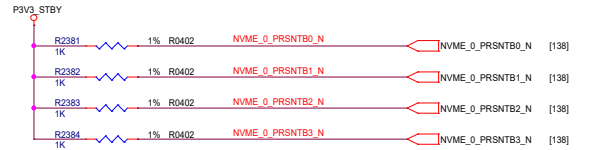
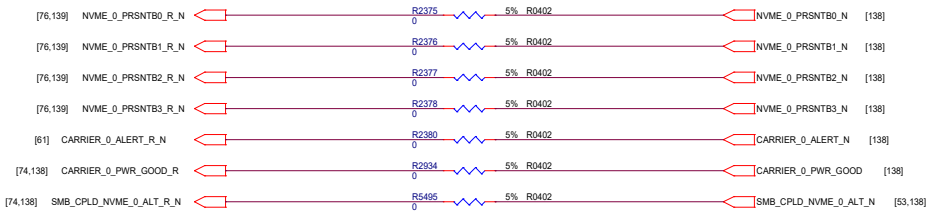


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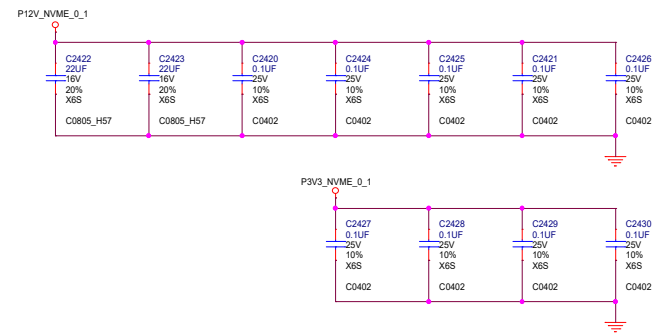
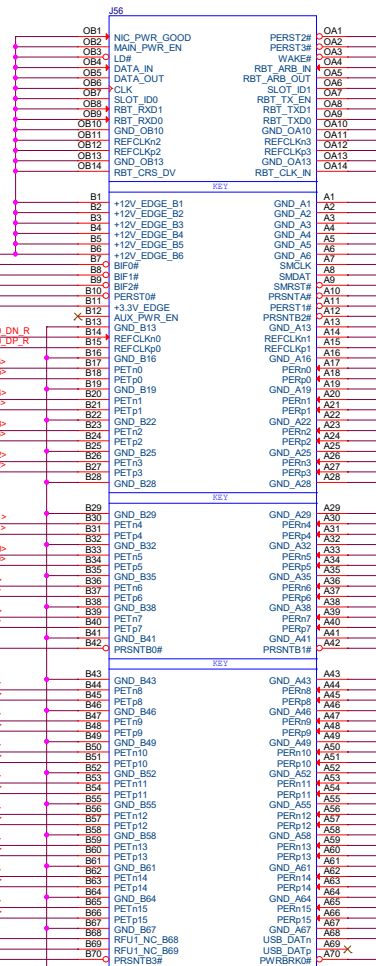
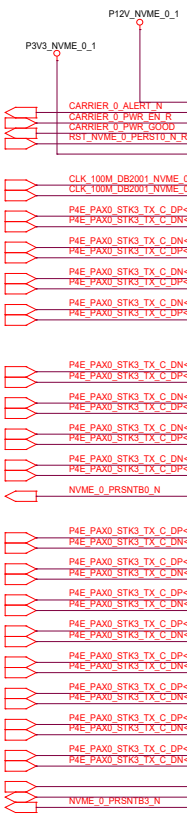
[138] CARRIER_0_ALERT_N
[74] CARRIER_0_PWR_GOOD
[138] CARRIER_0_PWR_GOOD
[139] RST_NVME_0_PERS10_N_R

[43] CLK_100M_DB2001_NVME_0_0_DN_R
[43] CLK_100M_DB2001_NVME_0_0_DP_R
[13] P4E_PAX0_STK3_TX_C_DP<15>
[13] P4E_PAX0_STK3_TX_C_DP<15>
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[13] P4E_PAX0_STK3_TX_C_DP<4>
[13] P4E_PAX0_STK3_TX_C_DP<3>
[13] P4E_PAX0_STK3_TX_C_DP<3>
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[13] P4E_PAX0_STK3_TX_C_DP<2>
[13] P4E_PAX0_STK3_TX_C_DP<1>
[13] P4E_PAX0_STK3_TX_C_DP<1>
[13] P4E_PAX0_STK3_TX_C_DP<0>
[13] P4E_PAX0_STK3_TX_C_DP<0>

[54,138] SMB_CPLD_NVME_0_R_SCL
[54,138] SMB_CPLD_NVME_0_R_SDA
[138] NVME_0_PRSNTB3_N



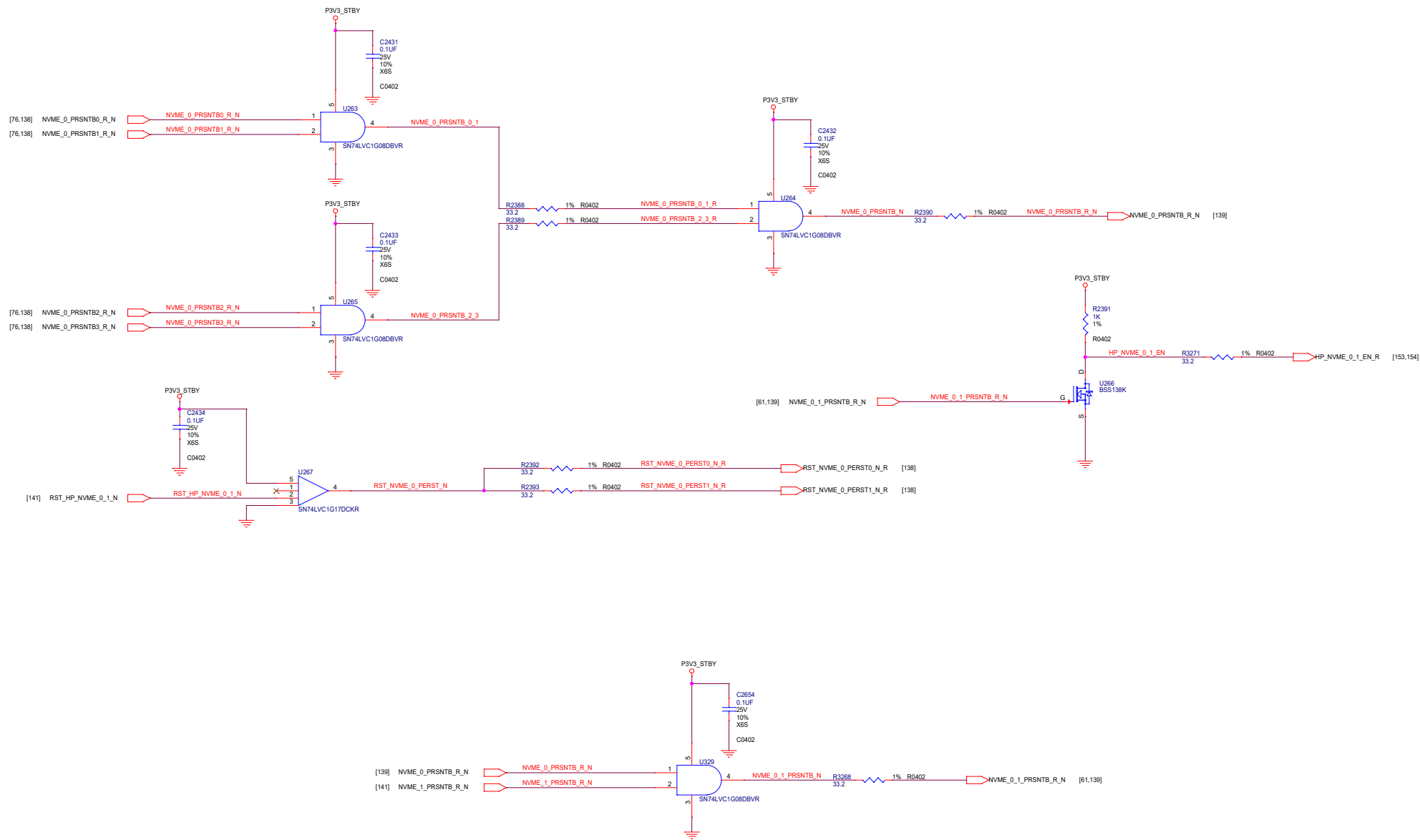
LANE REVERSAL POLARITY REVERSAL (TX<0> ~ <7>, TX<15>) PRIMARY CONNECTOR

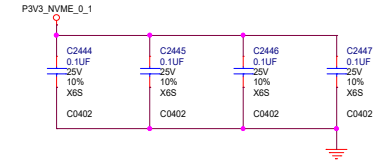
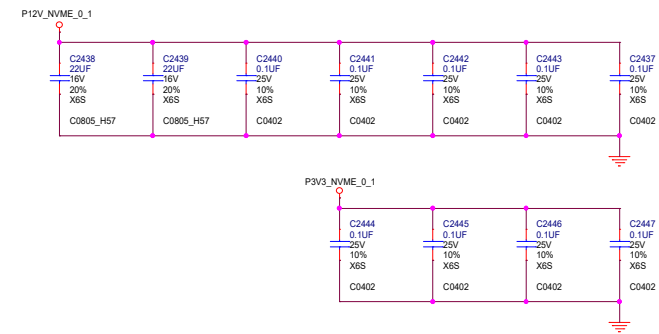


PCIE_NVME_0(1/2)

SCONN168_ME1016810202011

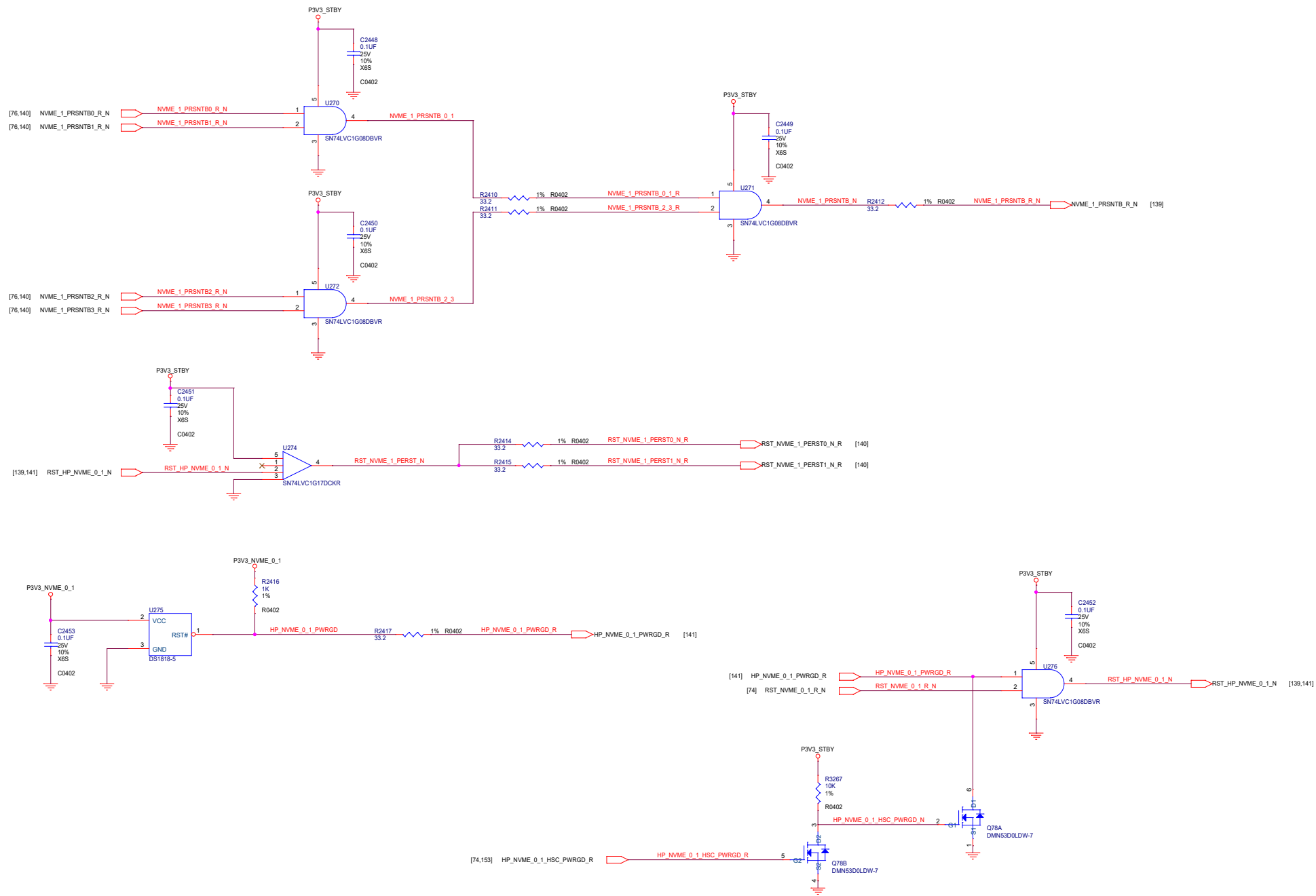
PCIE_NVME_0(2/2)

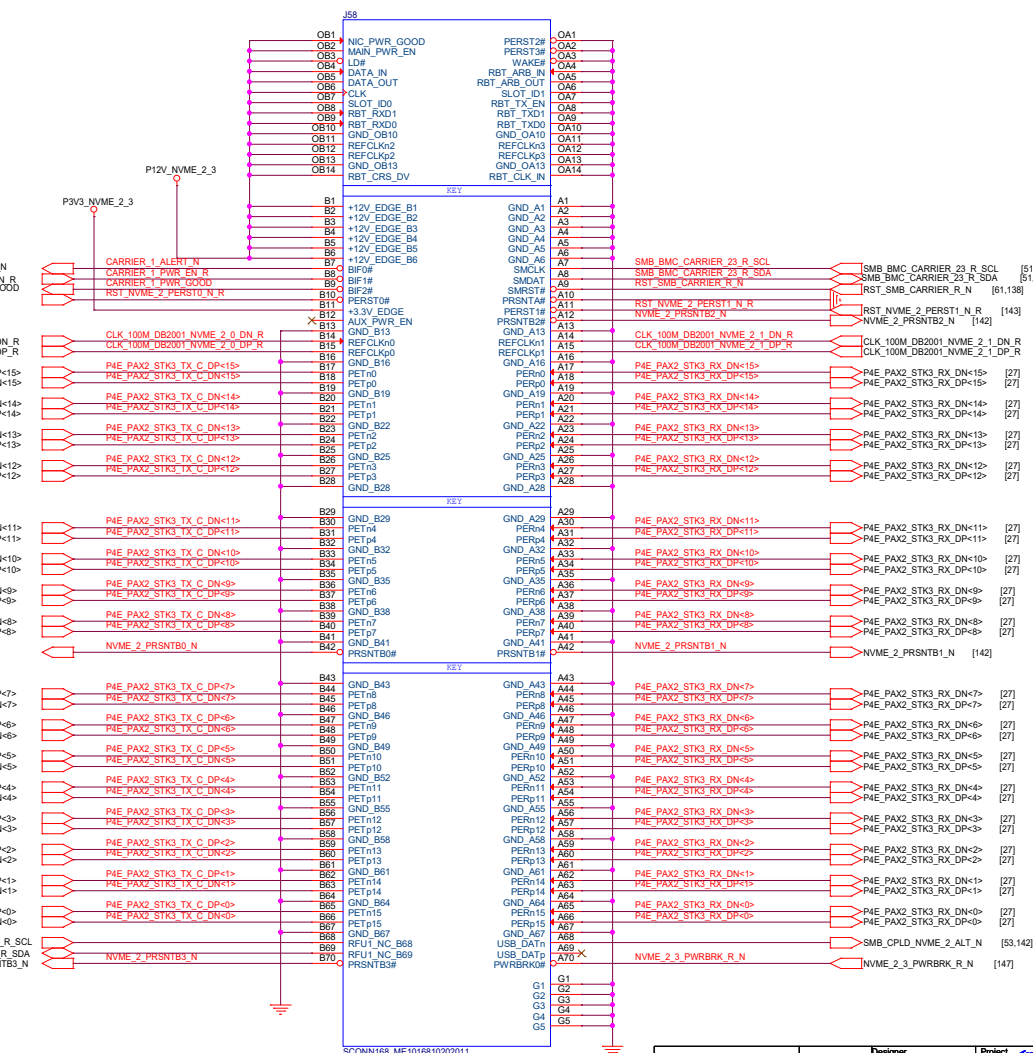
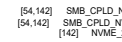
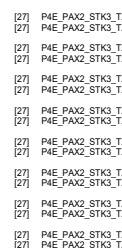
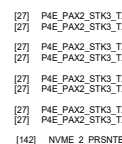
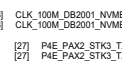
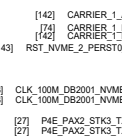
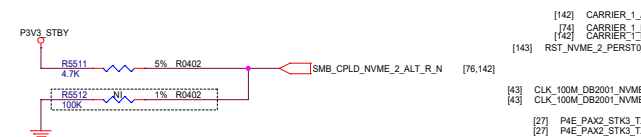
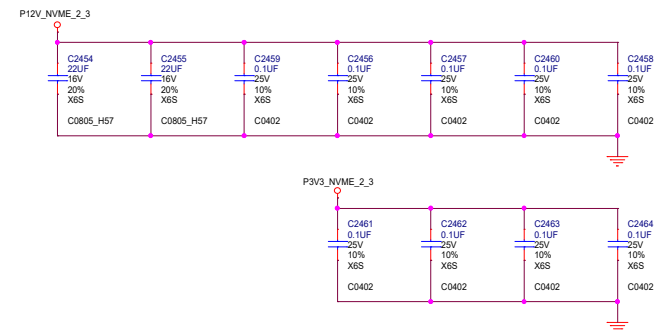


[illegible]

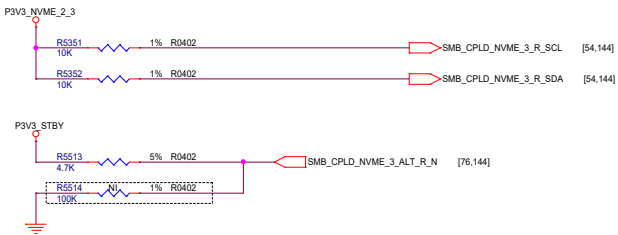
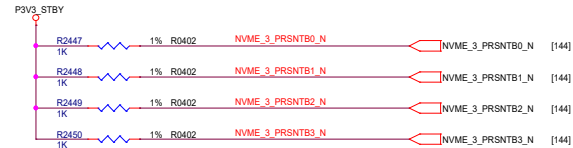
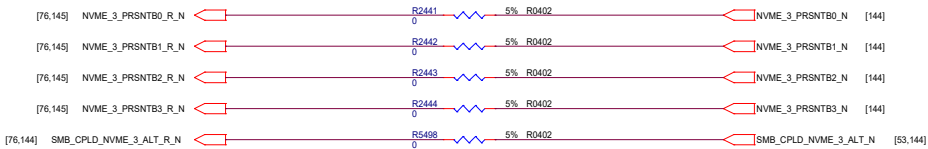
SCONN168 ME101681020201

PCIE_NVME_1(2/2)





LANE REVERSAL
POLARITY REVERSAL (TX<0> ~ <7>, TX<15>)
PRIMARY CONNECTOR



[145] RST_NVME_3_PERST0_N_R

[43] CLK_100M_DB2001_NVME_3_0_DN_R
[43] CLK_100M_DB2001_NVME_3_0_DP_R

[34] P4E_PAX3_STK3_TX_C_DP<15>
[34] P4E_PAX3_STK3_TX_C_DP<15>
[34] P4E_PAX3_STK3_TX_C_DP<14>
[34] P4E_PAX3_STK3_TX_C_DP<14>
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[144] NVME_3_PRSNTB0_N

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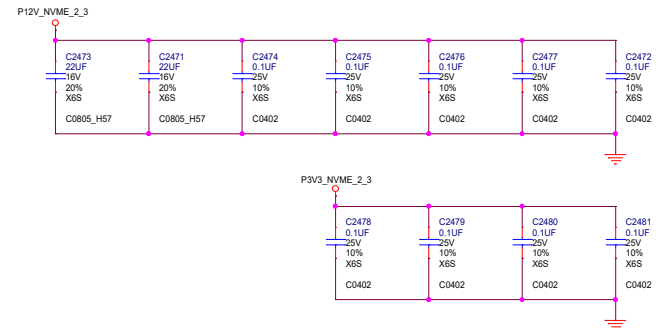
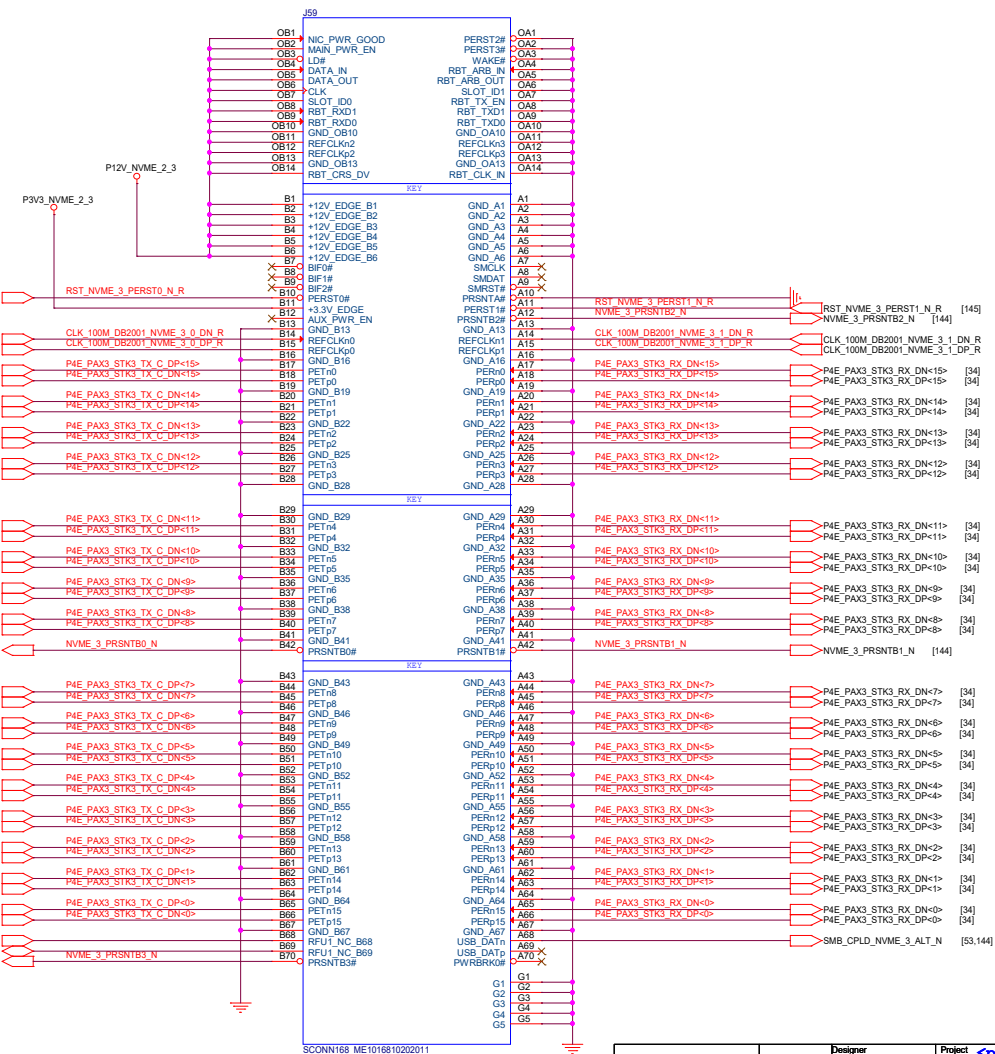
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[34] P4E_PAX3_STK3_TX_C_DP<3>

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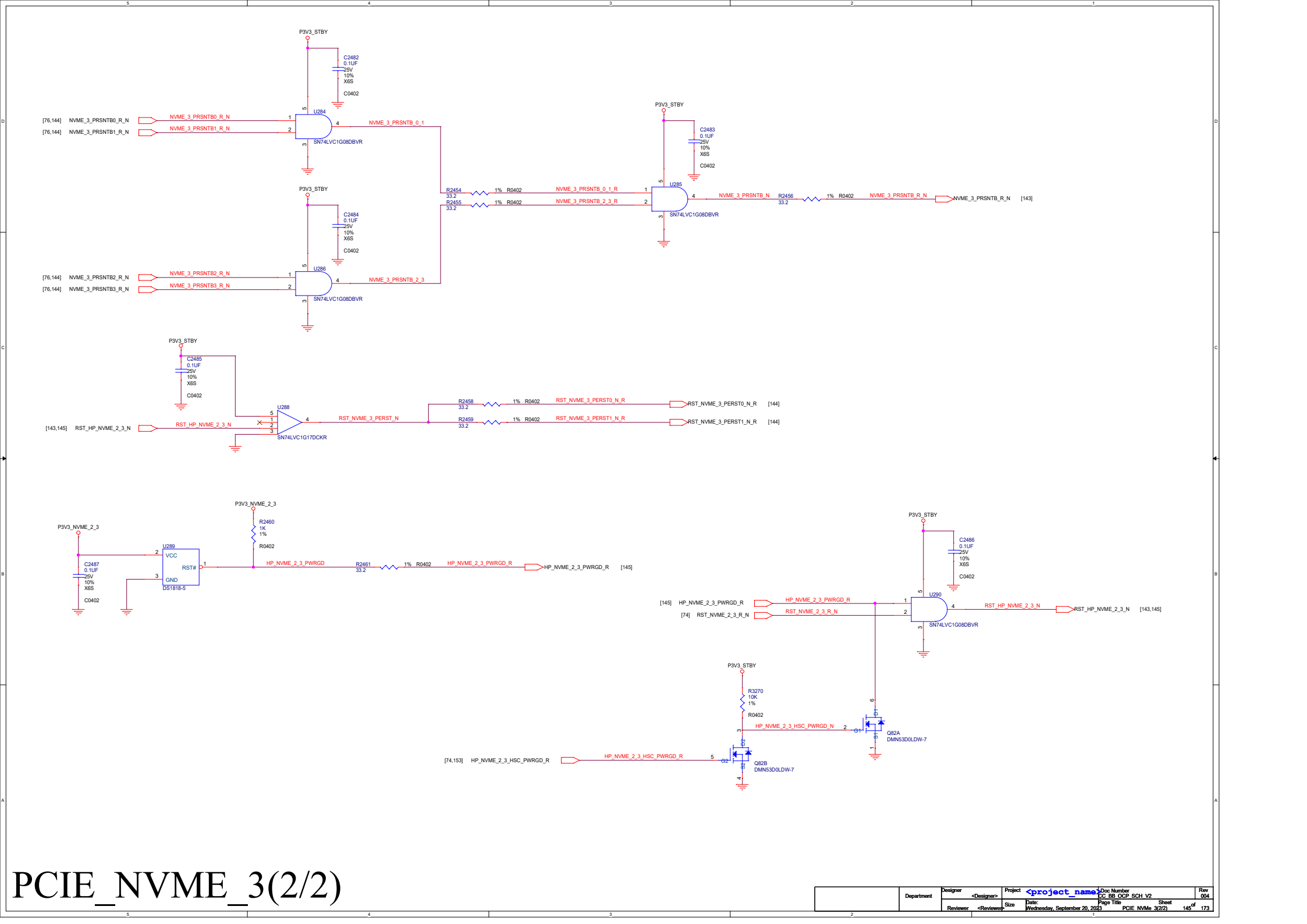
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[54,144] SMB_CPLD_NVME_3_R_SCL
[54,144] SMB_CPLD_NVME_3_R_SDA
[144] NVME_3_PRSNTB3_N

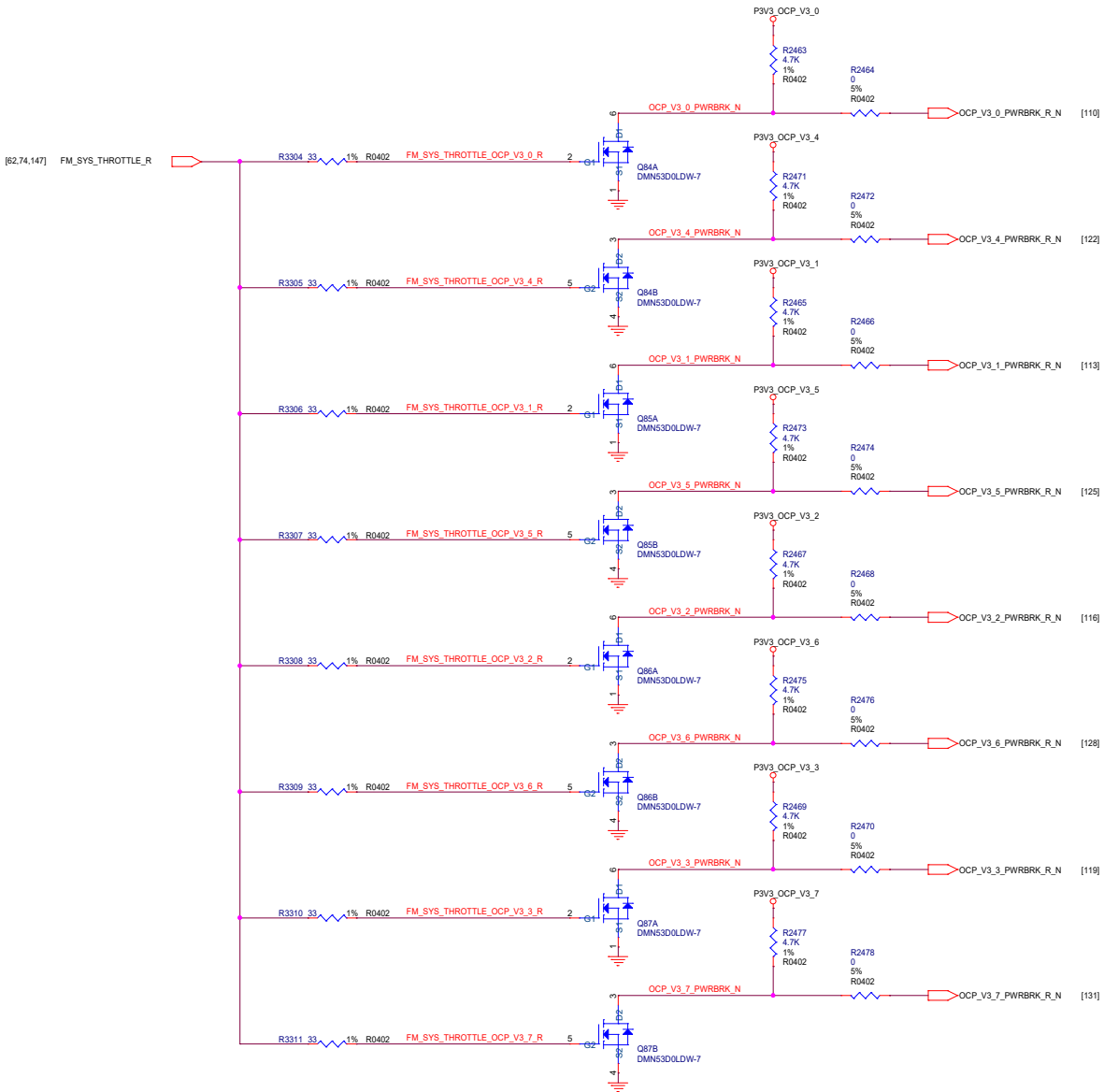
LANE REVERSAL POLARITY REVERSAL (TX<0> ~ <7>, TX<15>) SECONDARY CONNECTOR



PCIE_NVME_3(1/2)



PCIE_NVME_3(2/2)



THROTTLE(1/2)

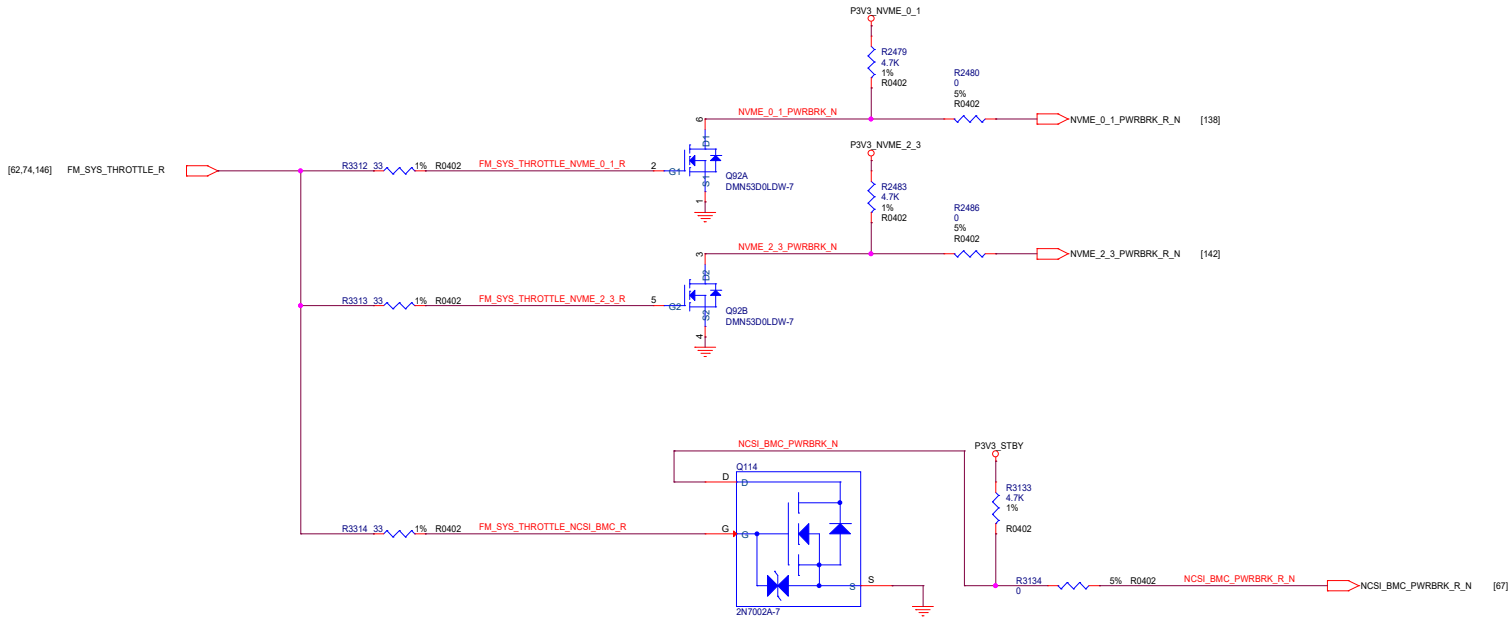
5 4 3 2 1

D

C

B

A



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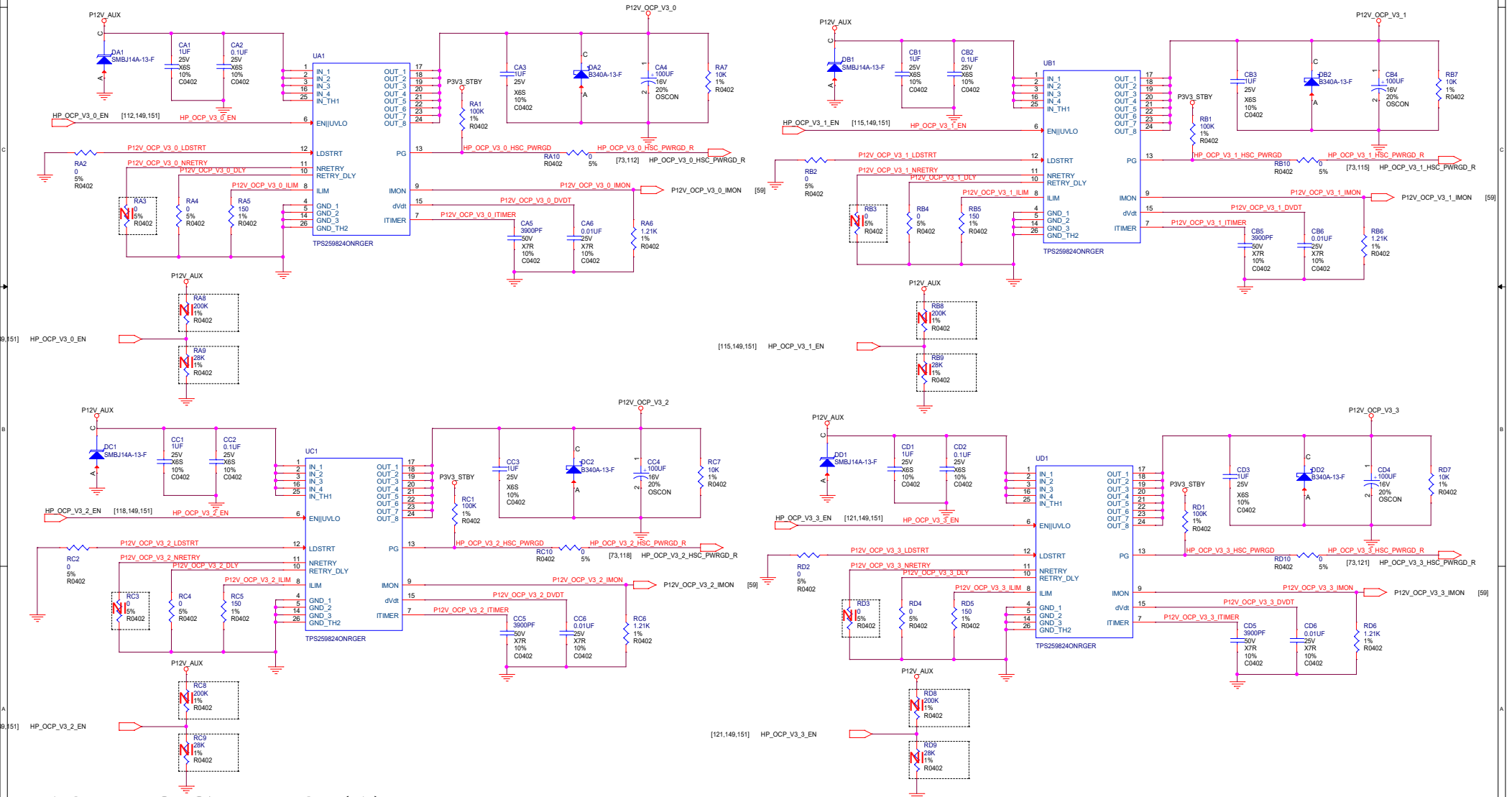
LDSTRT:
GND=disable the LDSTRT function

Current scale setting
1.21K Ohms sets 300mV/A
Output voltage slew rate setting
10nF sets 0.46V/ms
4.7nF sets 1V/ms
3.3nF sets 1.4V/ms

ITIMER setting
3.9nF sets 2 ms delay
47nF sets 20 ms delay

P12V_TOLERANCE +/-8% (SFP08T80K)
T02C0A30=4.6A
ID: NC08=50mA (MAX)
OCP= 9.84A

RETRY_DLY	NRETRY	DEVICE STATE
Short to GND	X	LATCH OFF
OPEN	open	4 auto-retries
OPEN	Short to GND	infinite number of retry



P12V_OCP_V3 (1)

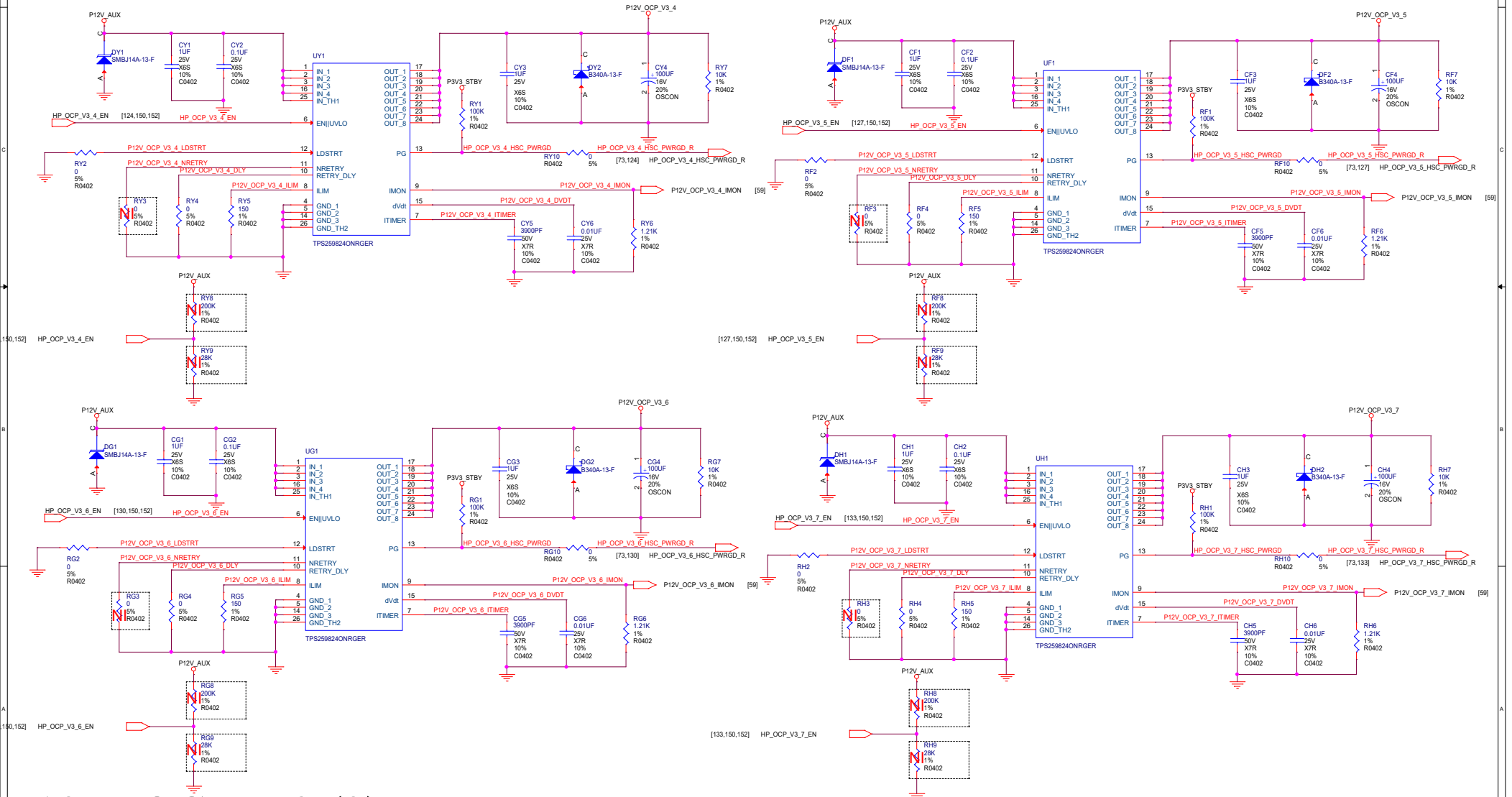
LDSTRT:
GND=disable the LDSTRT function

Current scale setting
1.21K Ohms sets 300mV/A
Output voltage slew rate setting
10nF sets 0.46V/ms
4.7nF sets 1V/ms
3.3nF sets 1.4V/ms

ITIMER setting
3.9nF sets 2 ms delay
47nF sets 20 ms delay

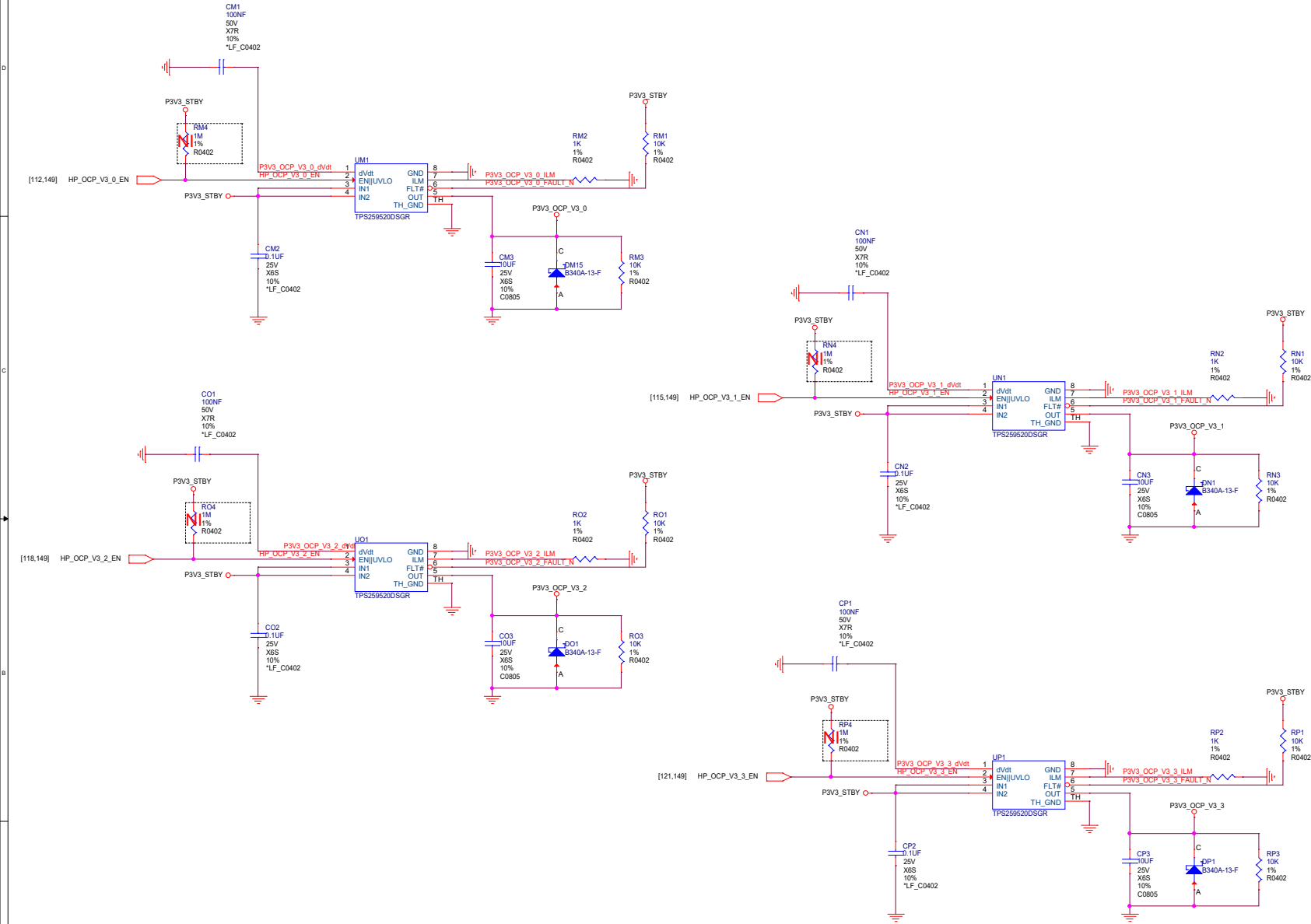
P12V_TOLERANCE +/-8% (SFP0820K)
T02C0A02=6.0A
ID: NC08=50mA (MAX)
OCP= 9.84A

RETRY_DLY	NRETRY	DEVICE STATE
Short to GND	X	LATCH OFF
OPEN	open	4 auto-retries
OPEN	Short to GND	infinite number of retry



P12V_OCP_V3 (2)

TDC=MAX=1.1A
OCP= 2.04A



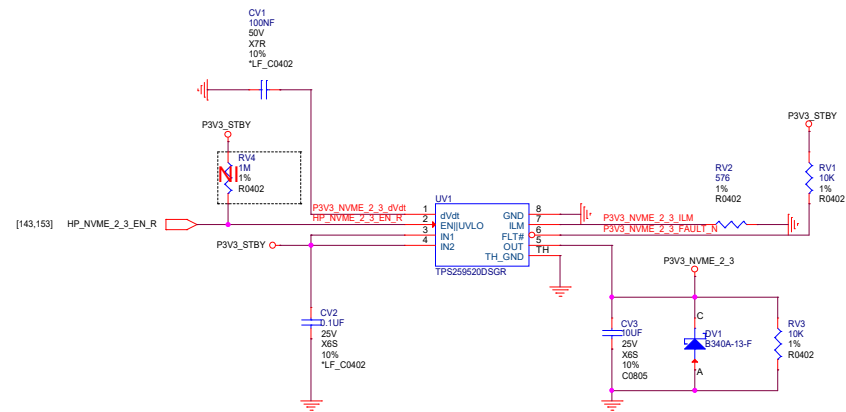
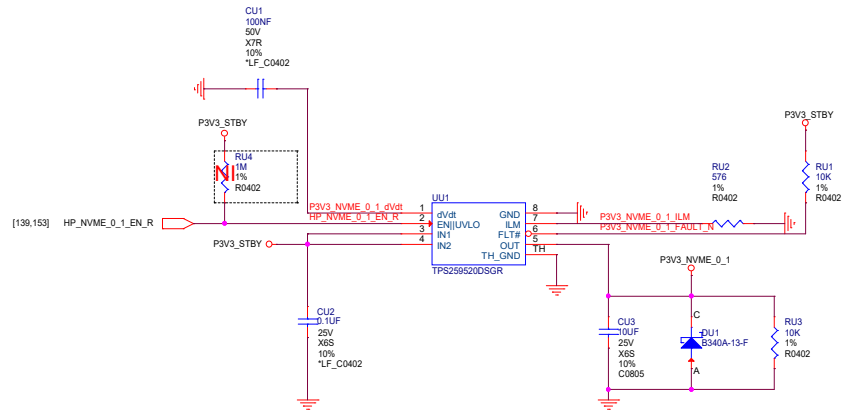
P3V3 OCP V3 (1)

NO	RADDR	Slave Address
1	2.49k	40h
2	7.5k	41h
3	12.4k	42h
4	17.4k	43h
5	24.9k	44h
6	34.8k	45h
7	47.5k	46h
8	63.4k	47h

5	24.9k	44h
6	34.8k	45h
7	47.5k	46h
8	63.4k	47h



TDC=MAX=2.2A
OCP= 3.58A



P3V3 NVME

Department	Designer	Project	Doc Number	Rev
	<Designer>	<project_name>	CC BB OCP SCH V2	004
	Reviewer	Size	Date:	Page Title
	<Reviewer>		Wednesday, September 20, 2023	P3V3 NVME 154 of 173

Output Voltage = 5V±5%
Output Ripple & Noise < 50mV
Transient Tolerance = ±250mV
TDC = 1.9A
Max current = 2.9A
Over-Current Protection(Max Rating x 1.3) = 3.77A
Current Step = 1.45A(TBD)
Slew Rate = 2.5A/us(TBD)
Work frequency = 1100kHz (Forced CCM)
Efficiency > 90% @TDC
COT Control Mode



Output Voltage = 3.3V±5%
Output Ripple & Noise < 50mV
Transient Tolerance = ±165mV
TDC = 11.31A
Max current = 12.729A
Over-Current Protection(Max Rating x 1.3) = 16.548A
Current Step = 6.3645A(TBD)
Slew Rate = 2.5A/us(TBD)
Work frequency = 600kHz(Forced CCM)
Efficiency > 90% @TDC
COT Control Mode



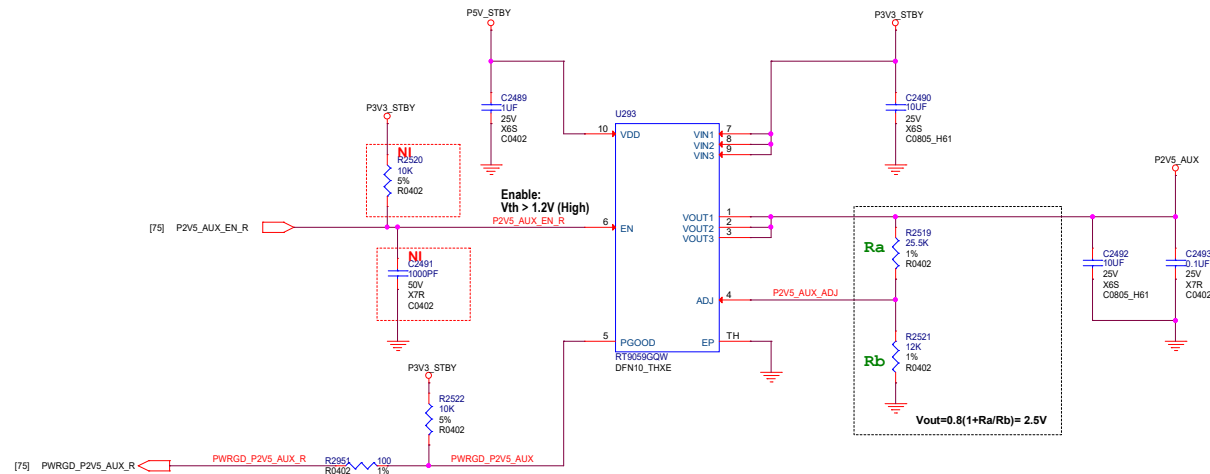
	Department	Designer	Project	Doc Number	Rev
		<Designer>	<project_name>	CC BB OCP SCH V2	004
		Reviewer	Size	Date:	Page Title
		<Reviewer>		Wednesday, September 20, 2023	VR P3V3 STBY
					Sheet 156 of 173

Vout = 2.5V
Vout Ripple & Noise < 50 mV (2%)
Vout Tolerance = +125 mV / -125 mV

Vout = 2.5V
Vout Ripple & Noise < 50 mV (2%)
Vout Tolerance = +125 mV / -125 mV

Iout MAX = 5 mA
 Iout OCP = 3.6 A (Spec)
 Load Step = 0.1 A (TBD)
 Slew Rate = 2.5A/us (TBD)

LDO
 $PD = (3.3 - 2.5) \times 0.005 = 0.003W$



P2V5_AUX

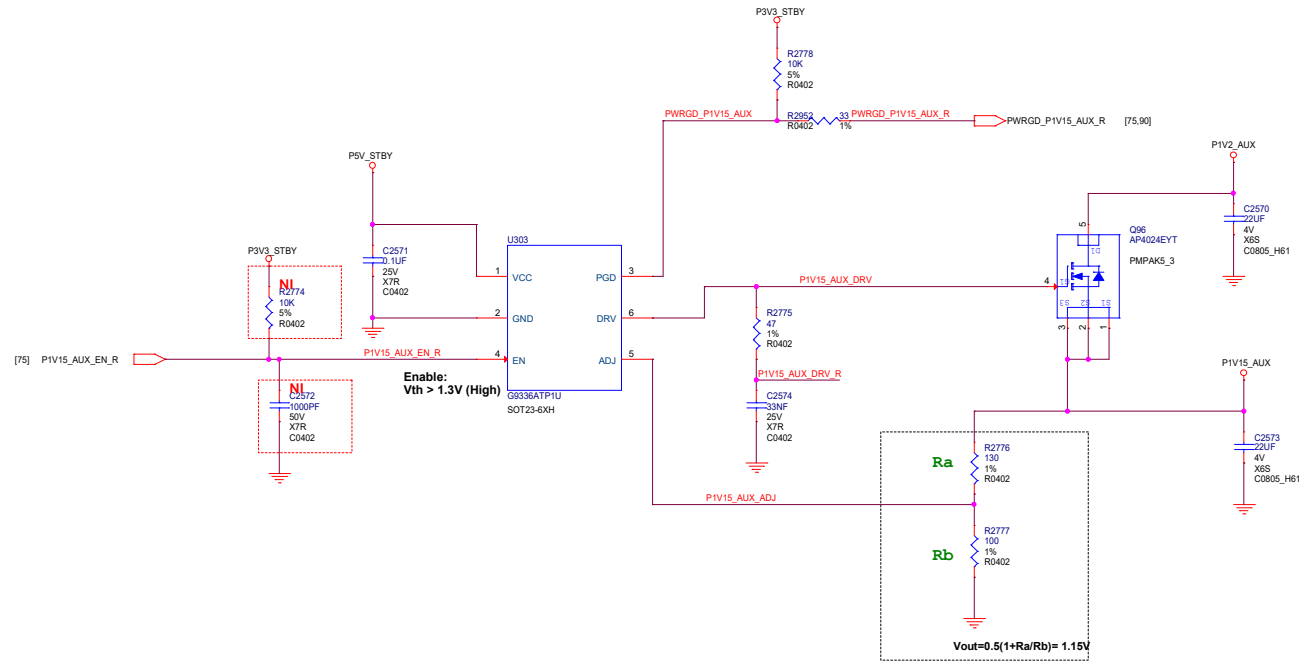
	Department	Designer	Project	Doc Number	Rev
		<Designer>	<project_name>	CC BB OCP SCH V2	004
		Reviewer	Size	Date:	Page Title
		<Reviewer>		Wednesday, September 20, 2023	VR P2V5 AUX
					Sheet 157 of 173

Design specification

Vout = 1.15 V
Vout Ripple & Noise < 50mV (4.3%)
Vout Tolerance = +57.5 mV / -57.5 mV

Iout TDC = 0.56A
Iout MAX = 0.7A
Load Step = 0.35A(TBD)
Slew Rate = 2.5A/us (TBD)

LDO
 $PD = (1.2 - 1.15) \cdot 0.7 = 0.035W$



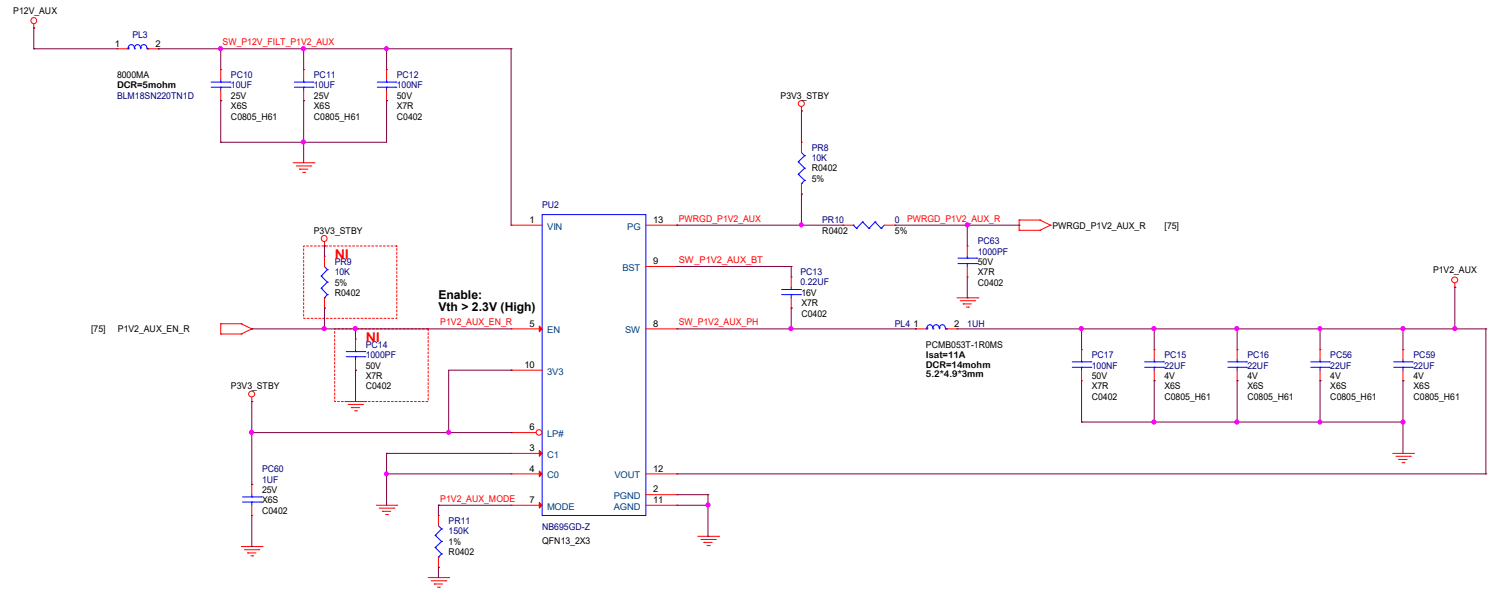
P1V15_AUX

Design specification

Vout = 1.2V
Vout Ripple & Noise < 50mV (4.1%)
Vout Tolerance = +60 mV / -60 mV

Iout TDC = 1.24A
Iout MAX = 1.48A
Iout OCP = 3.5A (Spec)
Load Step = 0.74A (TBD)
Slew Rate = 2.5A/us (TBD)

Fsw = 750k Hz
Efficiency > 85% @TDC
COT Control Mode



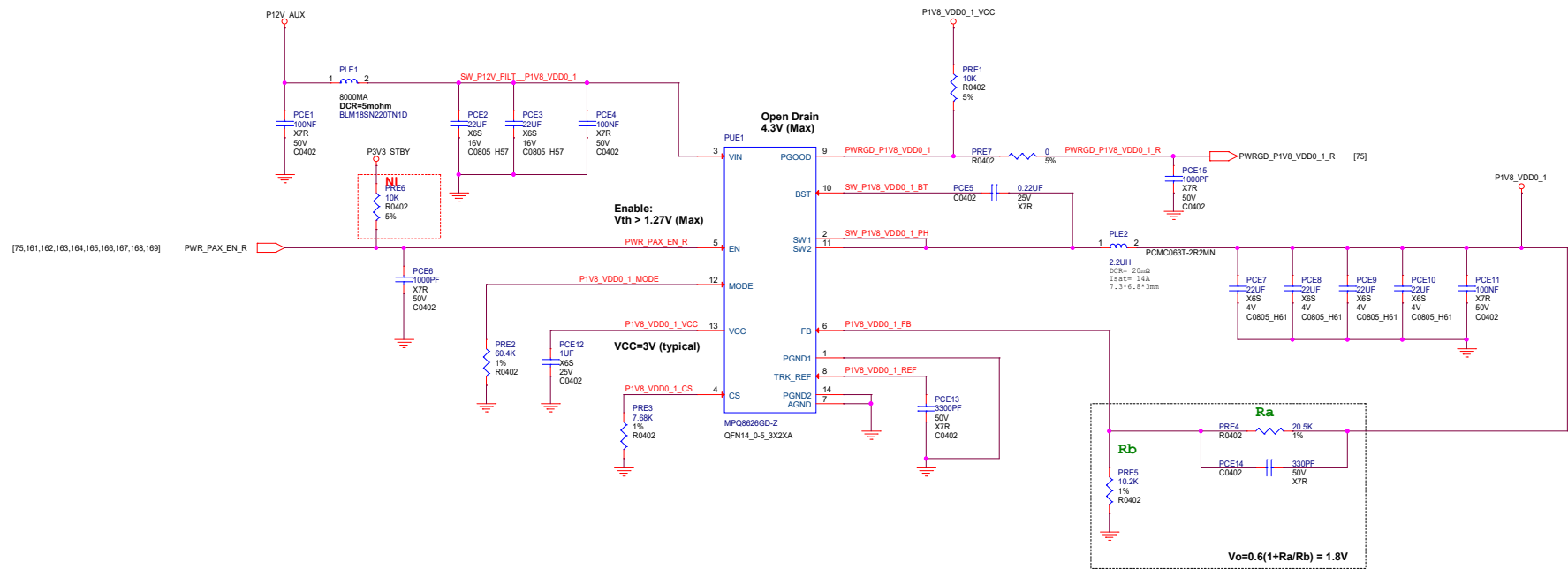
P1V2_AUX

Design specification

Vout = 1.8 V
Vout Ripple & Noise < 90 mV (5%)
Vout Tolerance = +45 mV / -45 mV

Iout TDC = 3.68A
Iout MAX = 3.68 A
Iout OCP = 4.4A
Load Step = 1.84 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 600k Hz (Forced CCM)
Efficiency > 85% @TDC
COT Control Mode



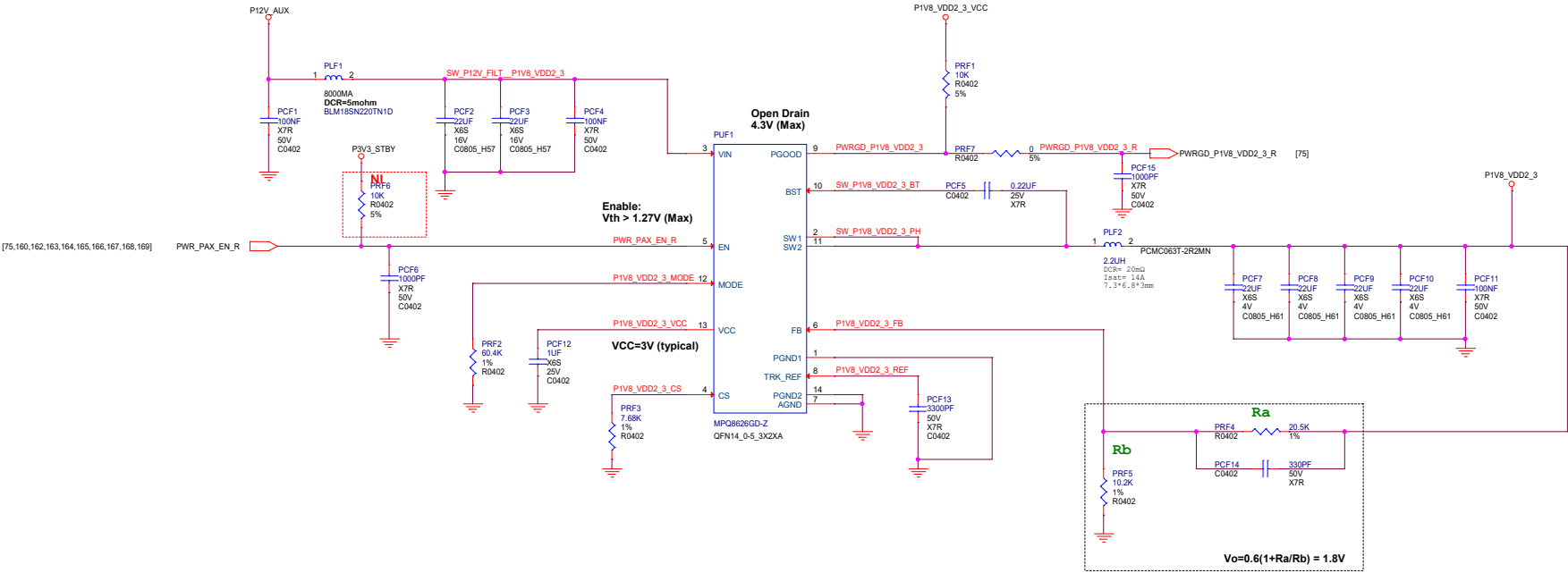
P1V8_VDD0_1

Design specification

Vout = 1.8 V
Vout Ripple & Noise < 90 mV (5%)
Vout Tolerance = +45 mV / -45 mV

Iout TDC = 3.68A
Iout MAX = 3.68 A
Iout OCP = 4.4A
Load Step = 1.84 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 600k Hz (Forced CCM)
Efficiency > 85% @TDC
COT Control Mode



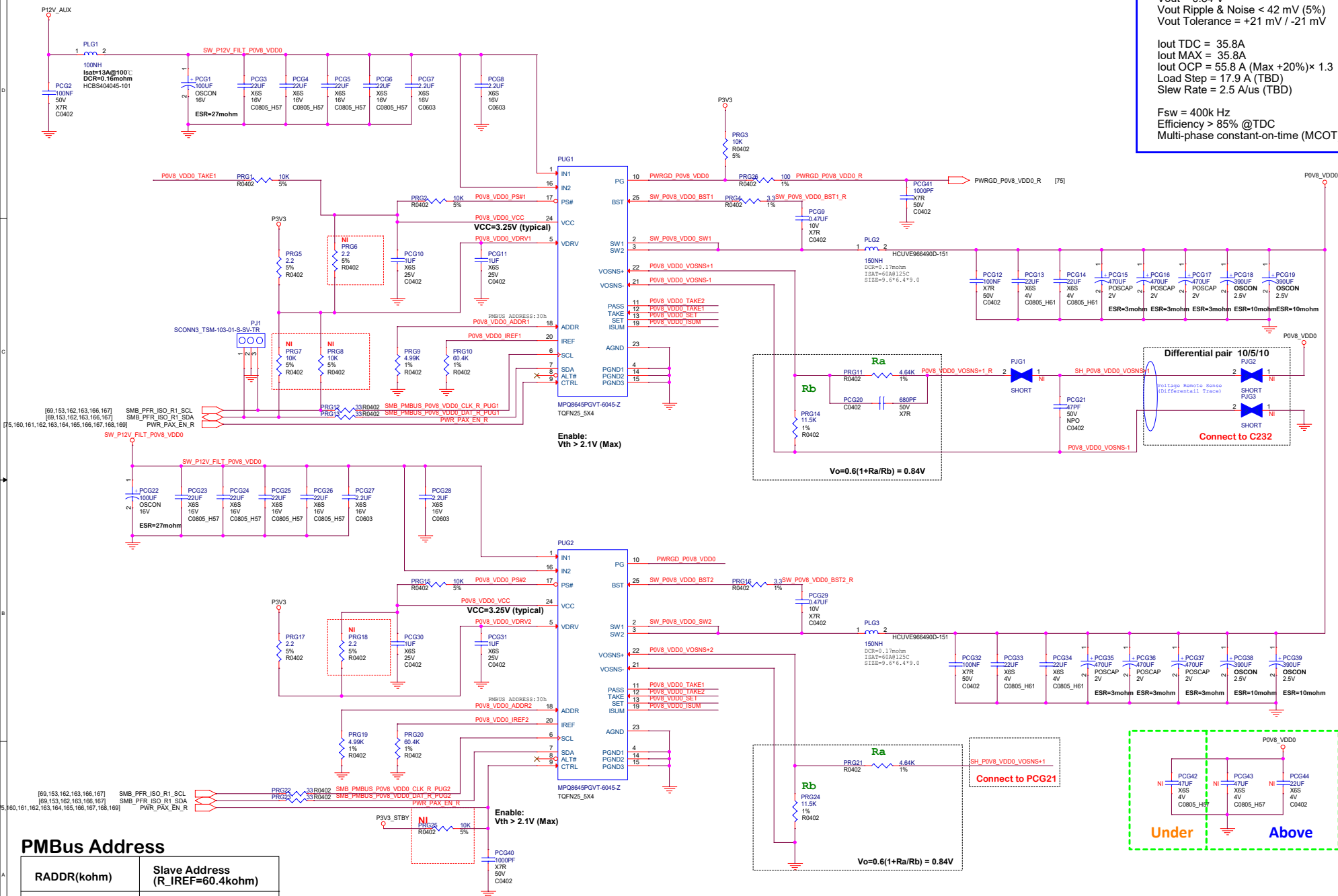
P1V8_VDD2_3

Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

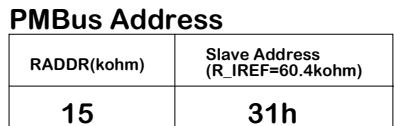
Iout TDC = 35.8A
Iout MAX = 35.8A
Iout OCP = 55.8 A (Max +20%) × 1.3
Load Step = 17.9 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 400k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



POV8_VDD0

Fsw = 400k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



	Department	Designer	Project	Doc Number	Rev
		<Designer>	<project_name>	CC BB OCP SCH V2	004
		Reviewer	Size	Date	Page Title
		<Reviewer>		Wednesday, September 20, 2023	VR P0V8 VDD1 163 of 173

Fsw = 400k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control

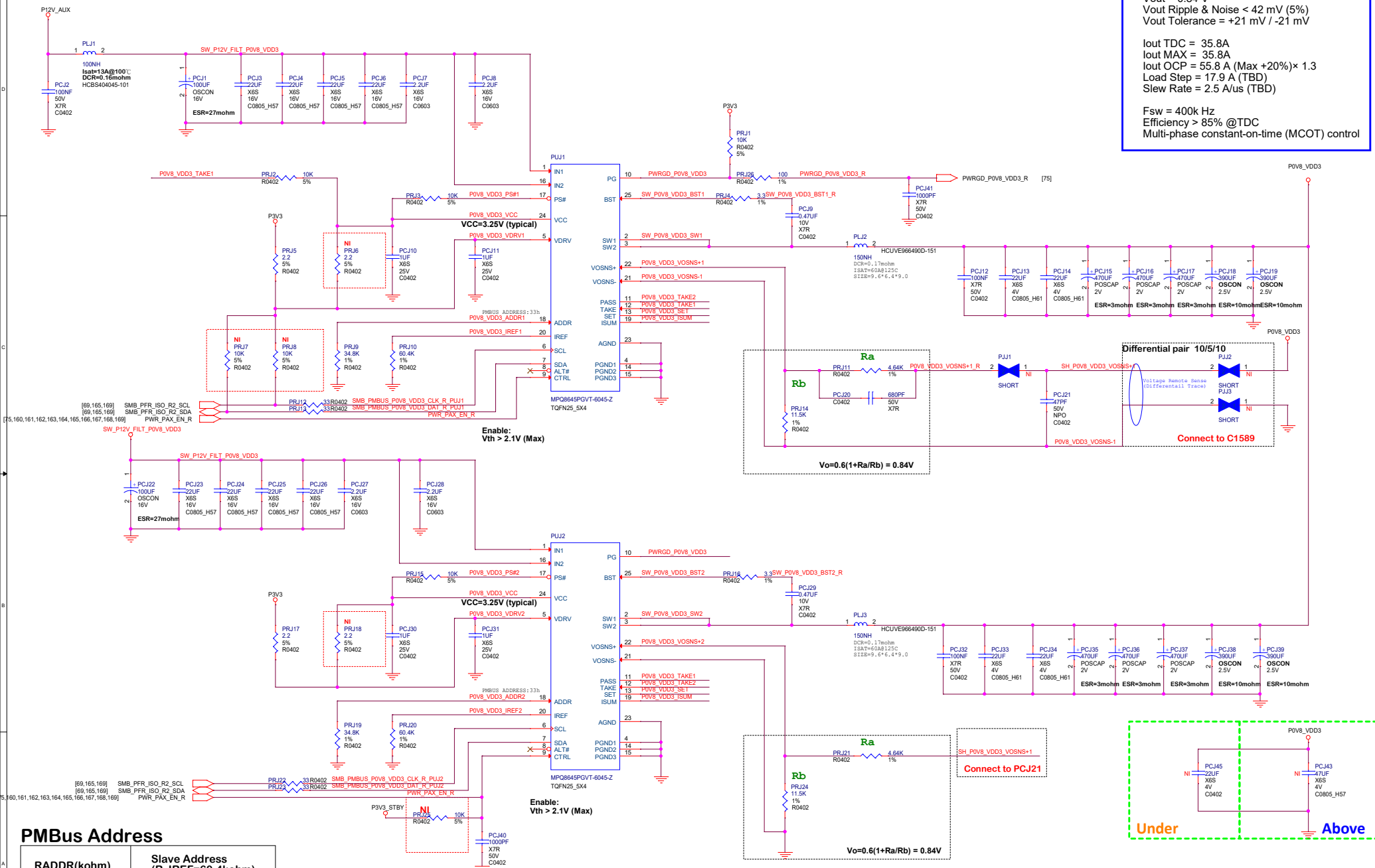


Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = 35.8A
Iout MAX = 35.8A
Iout OCP = 55.8 A (Max +20%) × 1.3
Load Step = 17.9 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 400k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



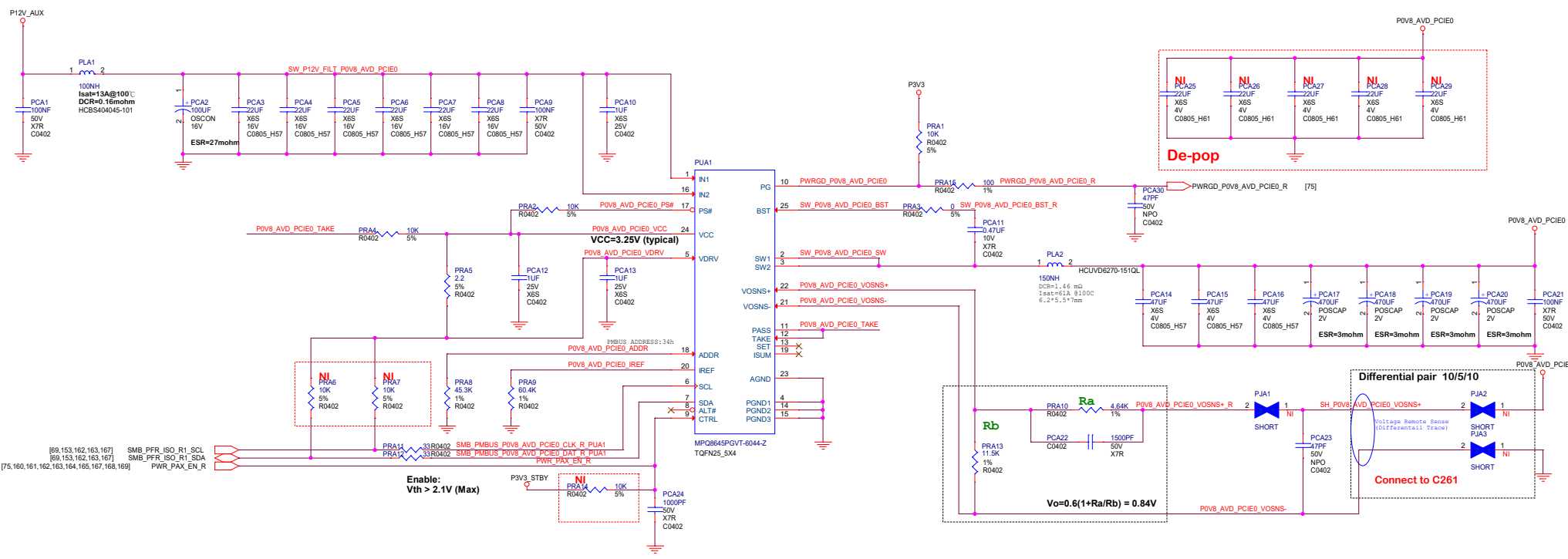
POV8_VDD3

Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = 13 A
Iout MAX = 13 A
Iout OCP = 16.9 A (Max × 1.3)
Load Step = 6.5 A (TBD)
Slew Rate = 2.5 A/μs (TBD)

Fsw = 600k Hz (Forced CCM)
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



PMBus Address

RADDR(kohm)	Slave Address (R_IREF=60.4kohm)
45.3	34h

P0V8_AVD_PCIE0

Design specification

Vout = 0.84 V

Vout Ripple & Noise < 42 mV (5%)

Vout Tolerance = +21 mV / -21 mV

Iout TDC = 13 A

Iout MAX = 13 A

Iout OCP = 16.9 A (Max × 1.3)

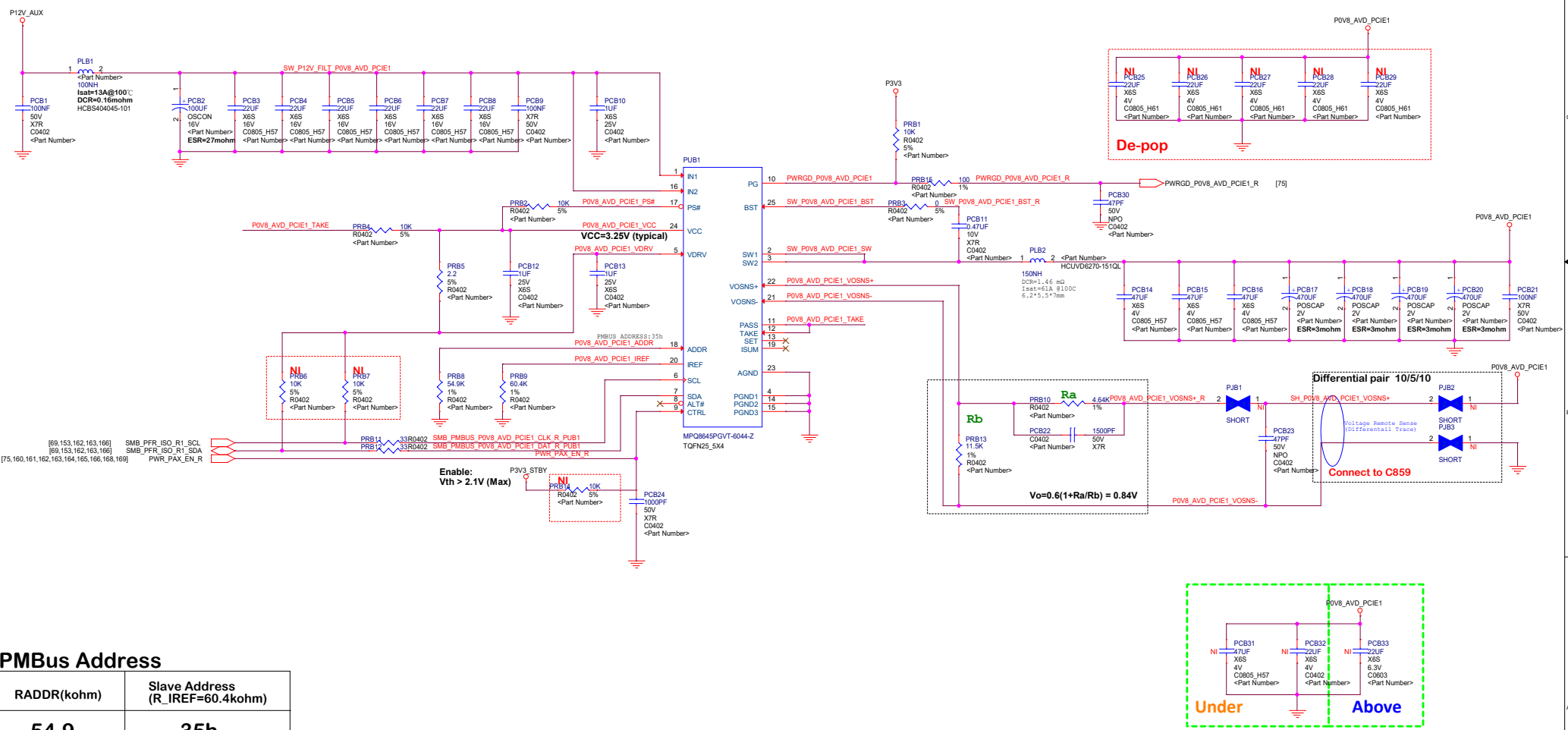
Load Step = 6.5 A (TBD)

Slew Rate = 2.5 A/μs (TBD)

Fsw = 600k Hz (Forced CCM)

Efficiency > 85% @TDC

Multi-phase constant-on-time (MCOT) control



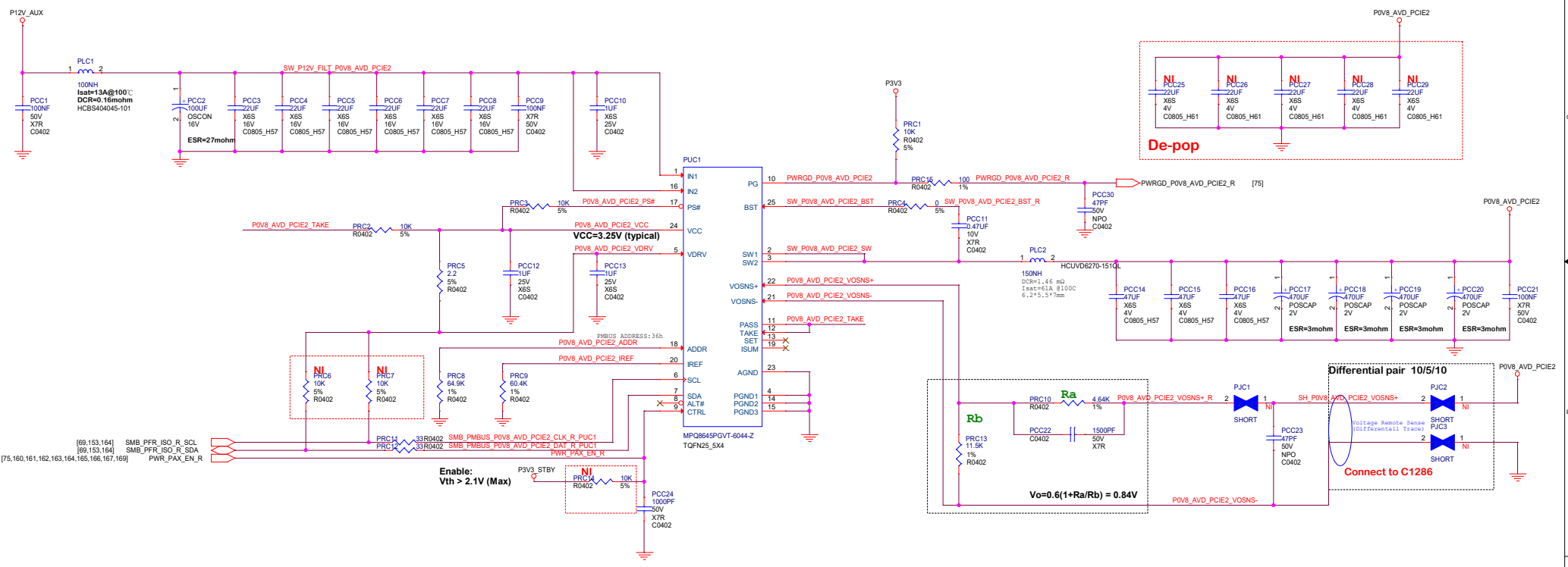
POV8_AVD_PCIE1

Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = 13 A
Iout MAX = 13 A
Iout OCP = 16.9 A (Max × 1.3)
Load Step = 6.5 A (TBD)
Slew Rate = 2.5 A/μs (TBD)

Fsw = 600k Hz (Forced CCM)
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



PMBus Address

RADDR(kohm)	Slave Address (R_IREF=60.4kohm)
64.9	36h

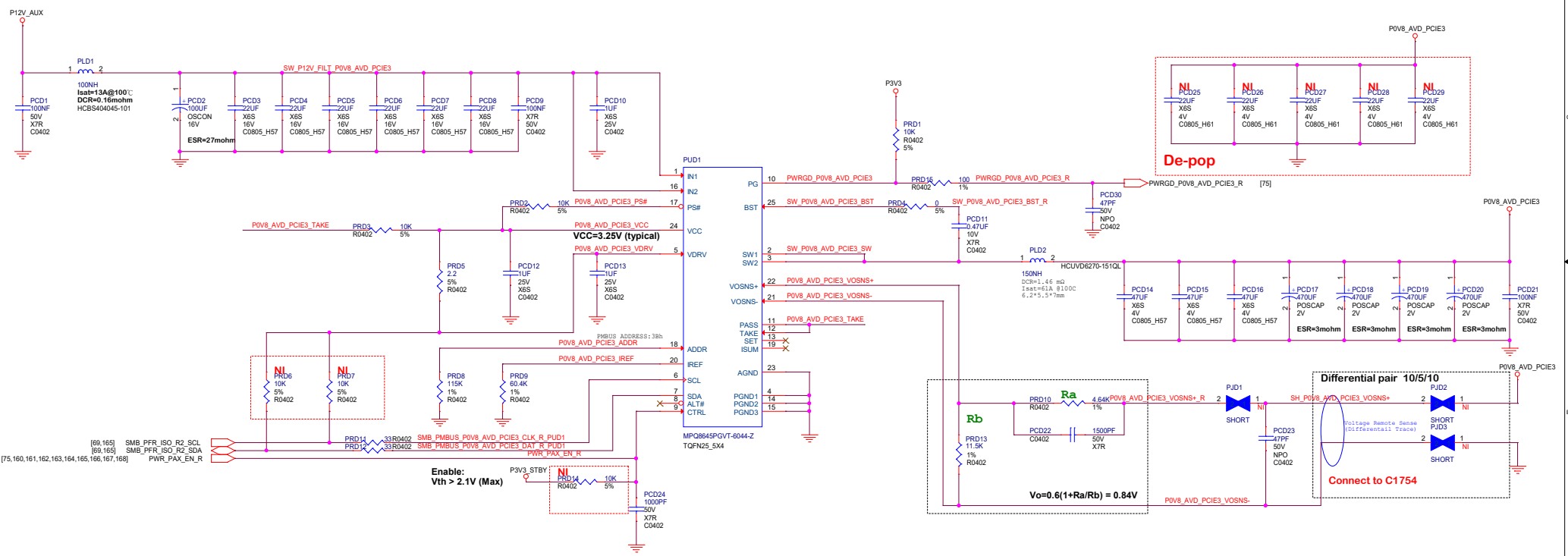
P0V8_AVD_PCIE2

Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = 13 A
Iout MAX = 13 A
Iout OCP = 16.9 A (Max × 1.3)
Load Step = 6.5 A (TBD)
Slew Rate = 2.5 A/μs (TBD)

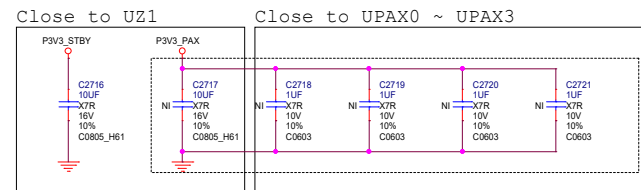
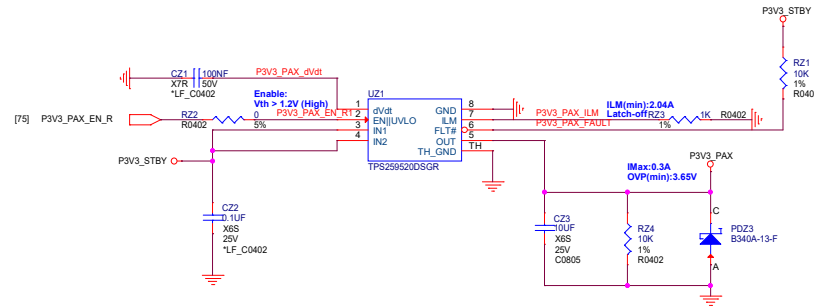
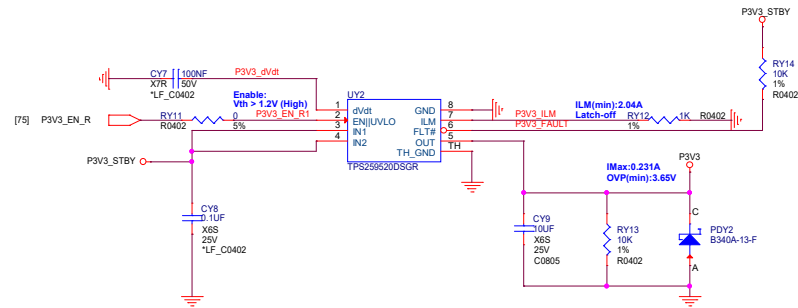
Fsw = 600k Hz (Forced CCM)
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



PMBus Address

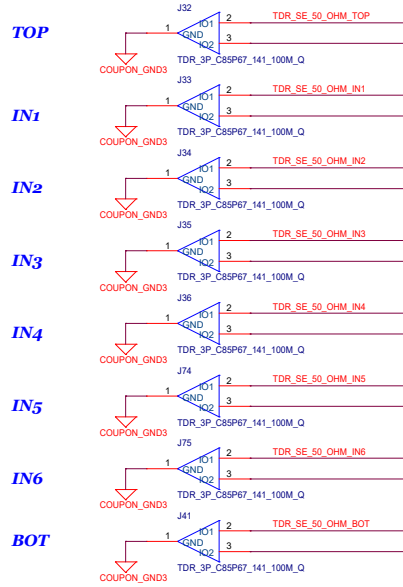
RADDR(kohm)	Slave Address (R_IREF=60.4kohm)
115	3Bh

P0V8_AVD_PCIE3

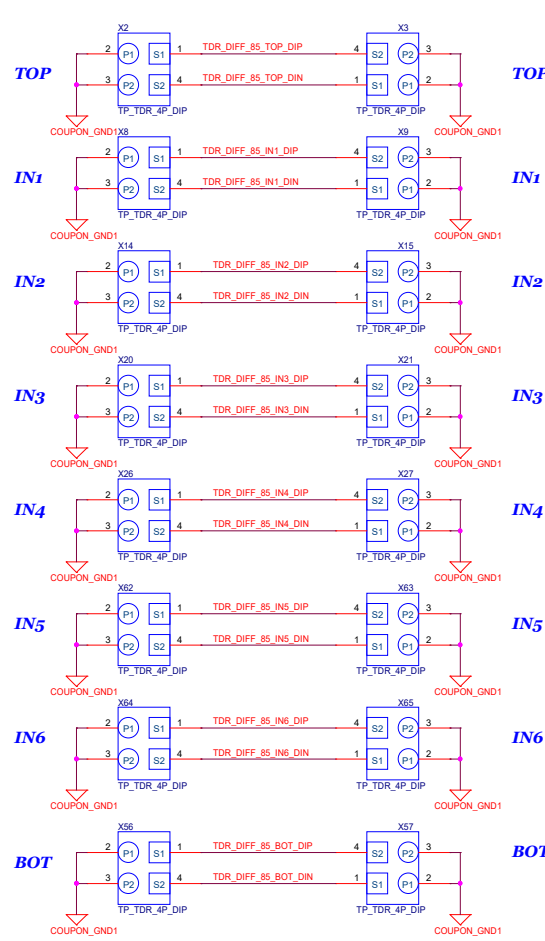


P3V3/P3V3_PAX

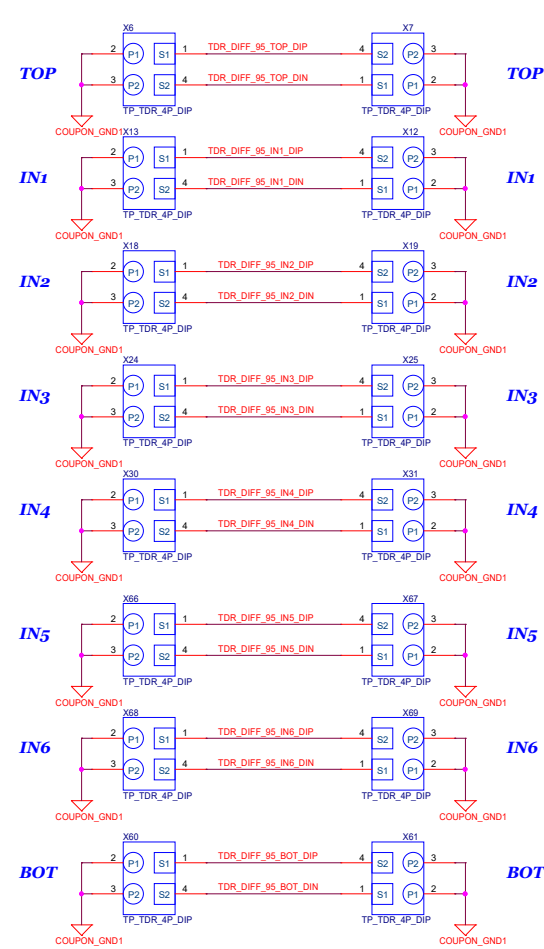
TDR-SINGLE



TDR-DIFFERENTIAL(85 ohm)

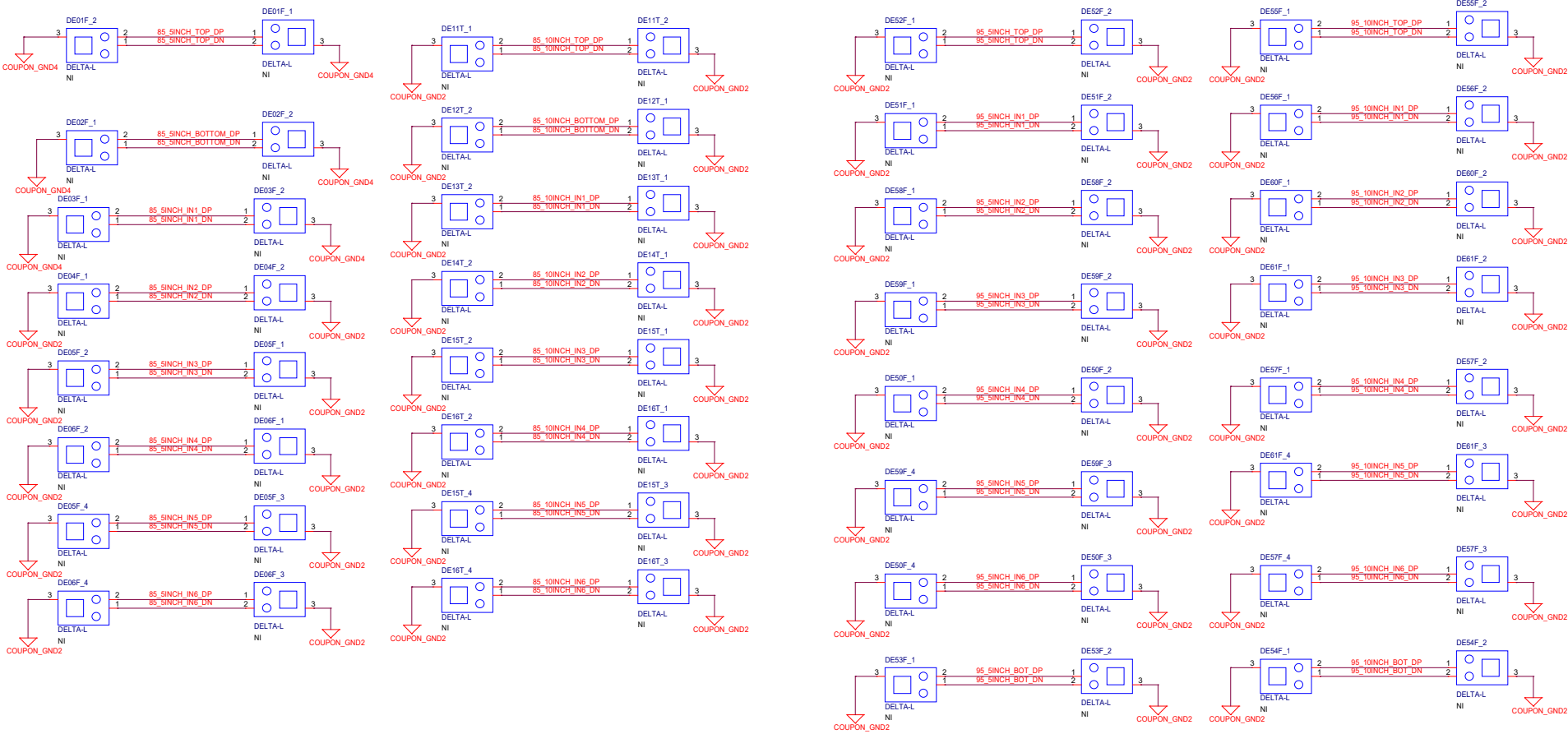


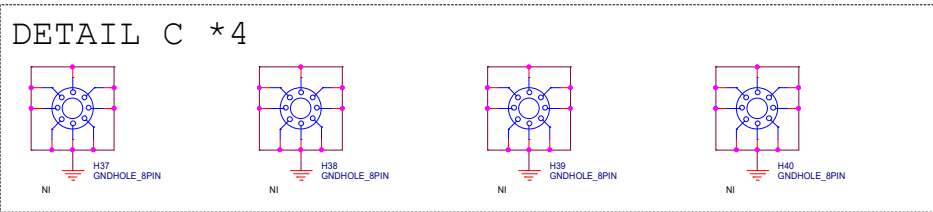
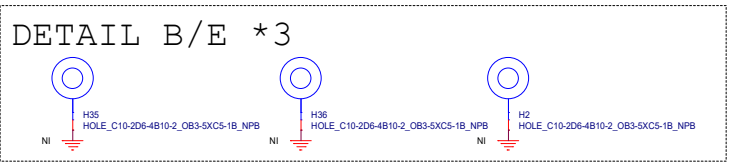
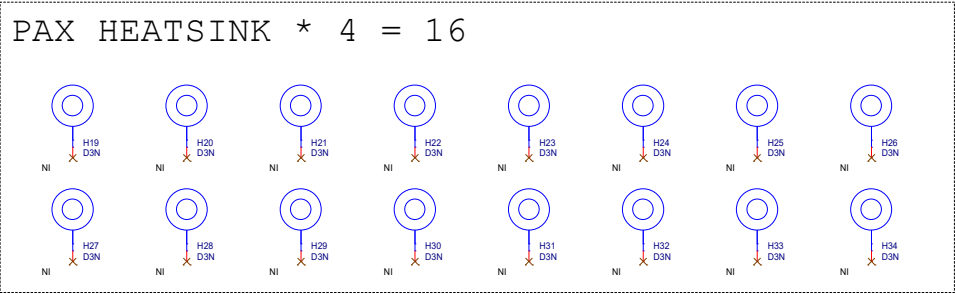
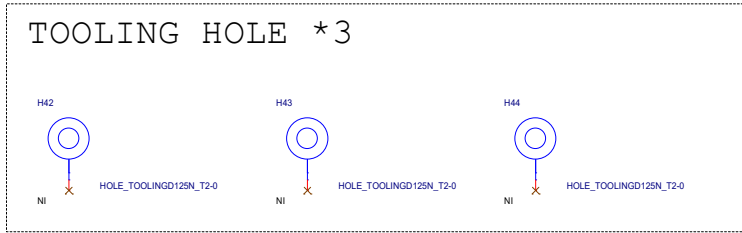
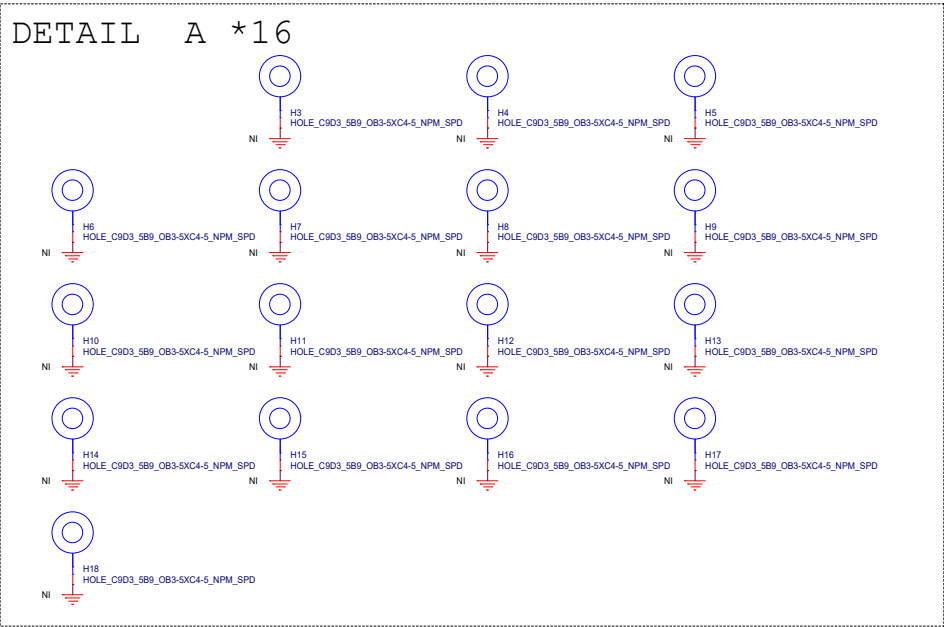
TDR-DIFFERENTIAL(95 ohm)



TDR

DELTA_L





SCREW HOLE